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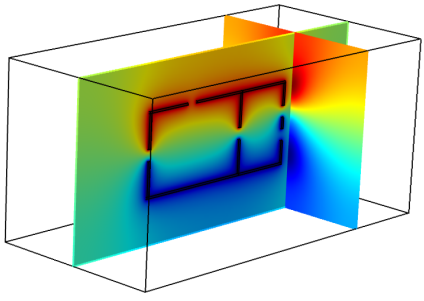
Hard- and Soft-Switching High-Frequency Power Electronics

Modelling of Parasitics and Electromagnetic Fields



Pieter Jacqmaer

Dissertation presented in partial fulfillment of the requirements for the degree of Doctor in Engineering Science

October 2015

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Doctoreren is niet alleen meten en theoretiseren. Af en toe moest er ook al

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Abstract

This work deals with increasing the switching frequency of transistors in power electronic converters. Higher switching frequencies lead to smaller passive components and this reduces the material cost and allows to meet space requirements more easily. In addition, faster converters respond more quickly to the changes of the controller signals. The facilitation of the increase of switching frequencies in power converters is therefore very important.

First, wide-bandgap semiconductors are studied. These are semiconductor materials that allow to reduce the dimensions of switching components with respect to silicon components for the same power capabilities. Therefore, they can switch faster and be operated at higher frequencies. A cooperation with Imec was started. Imec developed gallium nitride HEMTs. Important electric characteristics of these devices are measured in this work and a figure of merit is determined in order to compare them with conventional components and with WBG-competitors. A new measuring circuit is developed in order to determine the dynamic on-resistance of HEMTs and MOSFETs.

Another way to increase the switching frequency is the application of resonant techniques. As a result, the switching losses can be kept low and silicon components can be operated at high switching frequencies and fast rise and fall times. An LLC-converter is designed and developed. The necessary and sufficient conditions for zero voltage switching are analysed. The optimum values of the elements in the resonant tank are determined. The parasitic elements of the transformer are incorporated in the resonant tank. An accurate high-frequency model is developed for the transformer and it is examined whether the use of an air core has advantages. A fast gate-driver is developed and built, capable to control a half-bridge. The losses are simulated and determined for each element of the converter separately. The converter is also constructed and its efficiency is measured.

In converters operating at high frequencies and with fast dv/dt's and di/dt's, the parasitics in the components and those of the copper PCB-tracks become important. Unwanted oscillations and overshoot can occur, and therefore, a method is used in this work to predict these phenomena: the Partial Element Equivalent Circuit method. This technique is extensively validated by comparison with measurement results and the results of other modelling techniques, and is subsequently applied to switching converters.

Oscillations, overshoot and signal distortion are not the only problems caused by high frequencies and fast components, also the emission of electromagnetic fields is problematic. These fields may interfere with electronics in the vicinity of the converter. A tool is therefore developed in this work for calculating these fields. It is validated by applying it to systems and antenna topologies for which analytical solutions exist. Then, the field calculation technique is used to obtain the radiated emissions in CISPR 22 EMC-tests of an inverted buck converter.

Beknopte samenvatting

Dit werk handelt over het verhogen van de frequenties waaraan de transistoren in vermogenelektronische convertoren schakelen. Hogere schakelfrequenties leiden tot kleinere passieve componenten, hetgeen de materiaalkost verlaagt en toelaat om gemakkelijker aan de eisen voor ruimtegebruik te voldoen. Daarnaast zullen convertoren sneller reageren op veranderende controlesignalen. Het verhogen van schakelfrequenties is dus zeer belangrijk.

Eerst worden wide-bandgap halfgeleiders nader bestudeerd. Deze halfgeleidermaterialen laten toe de afmetingen van componenten te verkleinen in vergelijking met silicium componenten met dezelfde vermogenspecificaties. Daardoor kunnen ze sneller aan hogere frequenties schakelen. Er werd samengewerkt met Imec dat galliumnitride HEMT's ontwikkelde. Daarvan worden elektrische karakteristieken opgemeten en een winstfactor wordt bepaald waarmee ze met klassieke en concurrerende WBG-componenten kunnen vergeleken worden. Er wordt eveneens een nieuw meetcircuit ontwikkeld om de dynamische aan-weerstand te bepalen.

Een andere manier om schakelfrequenties te verhogen is het toepassen van resonante technieken. Daardoor worden de schakelverliezen laag gehouden en kunnen silicium componenten aan hoge frequenties uitgebaat worden. Een LLC-omvormer wordt ontworpen. De nodige en voldoende voorwaarden voor zero voltage switching worden geanalyseerd. De optimale waarden van de elementen van de resonante tank worden bepaald. De parasitaire elementen van een transformator worden geïncorporeerd in de resonante tank. Een nauwkeurig hoogfrequent model wordt opgesteld voor deze transformator en er wordt onderzocht of het gebruik van een luchtkern voordelen biedt. Een snelle gate-driver wordt ontwikkeld voor een halve brug. De verliezen worden gesimuleerd en bepaald per element van de convertor. De convertor wordt gebouwd en de efficiëntie wordt opgemeten.

In convertoren die werken aan hogere frequenties worden de parasitairen in de componenten en deze van de koperen PCB-banen, belangrijk. Ongewenste oscillaties en overshoot kunnen optreden. Daarom wordt er in dit doctoraatswerk een methode uitgewerkt om deze effecten te voorspellen: de Partial Element Equivalent Circuit methode. Deze wordt uitvoerig gevalideerd door de resultaten te vergelijken met meetresultaten en de resultaten die andere modelleringstechnieken geven. Daarna wordt de methode toegepast op schakelende convertoren.

Oscillaties, overshoot en signaalvervorming zijn niet de enige problemen die veroorzaakt worden door hoge frequenties en snelle componenten; ook de uitstraling van elektromagnetische velden is problematisch. Deze kunnen elektronica in de nabijheid van de convertor storen. Er wordt een tool ontwikkeld om deze velden te berekenen. Ze wordt gevalideerd door haar toe te passen op systemen en antennetopologieën waarvoor analytische oplossingen bestaan. Daarna wordt de veldberekeningsmethode op de CISPR 22 EMC-testen van een omgekeerde buck-convertor toegepast.

List of Abbreviations

AC	alternating current
BHFFOM	Baliga's high-frequency figure of merit
BiCMOS	bipolar complementary metal-oxide-semiconductor
BJT	bipolar junction transistor
BOM	bill of materials
CCM	continuous conduction mode
cf.	confer, see
ch.	chapter
CMOS	complimentary metal-oxide-semiconductor
coord.	coordinate
DC	direct current
DCM	discontinuous conduction mode
DDE	delay differential equation
DHFET	double-heterostructure field effect transistor
EFIE	electric field integral equation
EMC	electromagnetic compatibility
EMI	electromagnetic interference
eq.	equation
ESL	equivalent series inductance

ESR	equivalent series resistance
FET	field effect transistor
FHA	first harmonic approximation
Fig.	figure
FOM	figure of merit
FR4	flame retardant 4
GaAs	gallium arsenide
GaN	gallium nitride
GUI	graphical user interface
HEMT	high electron mobility transistor
HF	high-frequency
IFT	inverse fourier transform
IGBT	insulated gate bipolar transistor
LED	light-emitting diode
MESFET	metal-semiconductor field effect transistor
MnZn	manganese zinc
MOCVD	metalorganic chemical vapour deposition
MoM	method of moments
MOSFET	metal-oxide-semiconductor field effect transistor
NA	not available, or not applicable
NiZn	nickel zinc
PCB	printed circuit board
PDIP	plastic dual in-line package
PEC	perfectly electrically conducting
PEEC	partial element equivalent circuit
PSpice	personal simulation program with integrated circuit emphasis
PWM	pulse width modulation

QR	quasi-resonant
RMS	root mean square
SiC	silicon carbide
SiGe	silicon germanium
SMD	surface-mounted device
SMPS	switched-mode power supply
Spice	simulation program with integrated circuit emphasis
THD	total harmonic distortion
TL	transmission line
TO	transistor outline
vs.	versus
WBG	wide-bandgap
XOR	exclusive or
ZCS	zero current switching
ZVS	zero voltage switching

List of symbols

Remarks: SI-units are used throughout this work, unless otherwise specified or implicated, either in the following list or in the text itself where the quantity occurs. If the units in the actual text itself conflict with those in following list, the units specified in the text have priority.

The abbreviation 'dep.' in the column containing the units means that the units exist but are dependent on the specific situation.

L, C, R and G can also represent the inductance, capacitance, resistance and conductance per unit length and then have as units respectively [H/m], [F/m], [Ω/m] and [S/m].

A	Area; Surface; Magnitude of the magnetic vector potential	[m^2]; [/]; [V.s/m]
$[A]$	Connectivity matrix of a PEEC circuit	$[/]_{((M)\times(N))}$
A_L	Permeance of a magnetic core	[H/$turns^2$]
B	Magnitude of the magnetic flux density	[T]
B_{sat}	Saturation value of the magnetic flux density	[T]
BV	Breakdown voltage	[V]
c	Speed of light in vacuum	[m/s]
C	Capacitance	[F]
C_{ds}	Drain-to-source capacitance of a MOSFET	[F]
C_{gd}	Gate-to-drain capacitance of a MOSFET	[F]
C_{gs}	Gate-to-source capacitance of a MOSFET	[F]
C_{iss}	Input capacitance of a MOSFET	[F]
Cp	Partial capacitance	[F]
C_{pr}	Parallel-resonant capacitance in a resonant tank	[F]
C_{oss}	Output capacitance of a MOSFET	[F]

C_r	Resonant capacitance in a resonant tank	[F]
C_{rss}	Reverse transfer capacitance of a MOSFET	[F]
$[C_s]$	Short-circuit capacitance matrix	$[\mathrm{F}]_{(N\times N)}$
C_{sr}	Series-resonant capacitance in a resonant tank	[F]
d	Depth; Length; Dipole moment; Diameter; Distance	[m]; [m]; [C·m]; [m]; [m]
$\vec{e}$	Unit vector	[(dep.,dep.,dep.)]
E	Magnitude of the electric field; Energy;	[V/m]; [J]
E_c	Electric breakdown field	[V/m]
E_g	Bandgap energy	[J]
$\vec{E}_i$	Incident electric field	[(V/m,V/m, V/m)]
$\vec{E}_s$	Scattered electric field	[(V/m,V/m, V/m)]
f	Frequency	[Hz]
f_0	Resonance frequency	[Hz]
f_r	Resonance frequency	[Hz]
f_s	Switching frequency	[Hz]
g	Transconductance	[S]
G	Transconductance	[S]
h	Heat transfer coefficient; Height; Length	$[\mathrm{W/(K\cdot m^2)}]$; [m]; [m]
H	Magnitude of the magnetic field; Height	[A/m]; [m]
i	Current; Imaginary Unit $\sqrt{-1}$; Iteration variable	[A]; [/]; [/]
I	Current	[A]
$[I]$	Vector containing the currents in the inductive branches of a PEEC-circuit	$[\mathrm{A}]_{(M\times 1)}$
I_{load}	Load current	[A]
i_μ	Magnetization current in a transformer	[A]
I_{out}	Output current	[A]
$[I_s]$	Vector containing the source currents injected in the inductive branches of a PEEC-circuit	$[\mathrm{A}]_{(M\times 1)}$
j	Current density; Imaginary unit $\sqrt{-1}$	$[\mathrm{A/m^2}]$; [/]
J	Magnitude of the current density	$[\mathrm{A/m^2}]$
k	Boltzmann's constant; Wave number; Proportionality constant; Iteration variable	$[\mathrm{m^2\cdot kg/(s^2\cdot K)}]$; $[\mathrm{m^{-1}}]$; [dep.]; [/]

K	Proportionality constant; Coupling coefficient between two inductances; Number of conductors in a PEEC-circuit	[dep.]; [/]; [/]
l	Length; Iteration variable	[m]; [/]
L	Length; Inductance; Linear operator	[m]; [H]; [dep.]
$[L]$	Partial inductance matrix in a PEEC-system	$[\mathrm{H}]_{(M\times 1)}$
L_1	Inductance of the primary winding of a transformer	[H]
$L_{lk,p}$	Primary leakage inductance of a transformer	[H]
$L_{lk,s}$	Secondary leakage inductance of a transformer	[H]
L_M	Magnetization inductance of a transformer	[H]
L_p	Parallel inductance in a resonant tank	[H]
Lp	Partial inductance	[H]
M	Voltage amplification factor of a resonant converter; Number of inductive volume cells in a PEEC-system	[/]; [/]
$[M]$	System matrix of a PEEC circuit	$[\mathrm{dep.}]_{((M+N)\times(M+N))}$
n	Transformation ratio; Iteration variable; emission coefficient of a diode	[/]; [/]; [/]
N_1	Number of primary windings of a transformer	[/]
N_2	Number of secondary windings of a transformer	[/]
N_D	n-type doping density	$[\mathrm{m}^{-3}]$
$nhinc$	Number of filaments in the height-direction in a conductor in FastHenry	[/]
n_p	Number of primary windings of a transformer	[/]
$nwinc$	Number of filaments of a conductor in the width-direction in FastHenry	[/]
P	Active power; Unit pulse function defined on an inductive subdivision	[W]; [/]
$[P]$	Matrix of the coefficients of potential	$[\mathrm{F}^{-1}]_{(N\times N)}$
P_{core}	Total power losses in a magnetic core	[W]
P_{cu}	Total power losses in a copper windings around a magnetic core	[W]
P_{loss}	Power loss in a semiconductor switch	[W]
P_{out}	Output power	[W]
P_V	Loss density in a magnetic core	$[\mathrm{W/m}^3]$
q	Elementary charge	[C]
Q	Charge; Quality factor	[C]; [/]
$[Q]$	Vector of charges	$[\mathrm{C}]_{N\times 1}$

Q_{ds}	Charge stored in the drain-to-source capacitance of a MOSFET	[C]
Q_{gd}	Miller charge of a transistor	[C]
Q_{gs}	Gate-to-source charge of a transistor	[C]
$Q_{g,sw}$	Total switching gate charge of a transistor	[C]
r	Distance	[m]
R	Resistance; Distance between a source of electromagnetic fields and an observation point	[Ω]; [m]
$[R]$	Resistance matrix of a PEEC-system	$[\Omega]_{(M\times M)}$
R_{AC}	Equivalent AC-resistance of the output rectifier, output filter and load, in a converter	[Ω]
R_{core}	Core resistance of a transformer	[Ω]
rh	Ratio of the heights of two adjacent filaments of a segmented conductor in FastHenry	[/]
R_{load}	Load resistance of a converter	[Ω]
R_p	Resistance of the primary winding of a transformer	[Ω]
$R_{on,dyn}$	Dynamic on-resistance of a transistor	[Ω]
$R_{on,stat}$	Static on-resistance of a diode or transistor	[Ω]
R_s	Resistance of the secondary winding of a transformer; Resistance of a voltage source	[Ω]; [Ω]
rw	Ratio of the widths of two adjacent filaments of a segmented conductor in FastHenry	[/]
s	Fourier variable $j\omega$ or Laplace variable $\sigma + j\omega$; Separation distance	$[(1/\mathrm{s}) + j\cdot\mathrm{rad/s}]$; [m]
S	Apparent power; Magnitude of the Poynting vector; Surface	[VA]; $[\mathrm{W/m^2}]$; [/]
t	Time; Thickness	[s]; [m]
T	Temperature; Period	[K]; [s]
T_a	Ambient temperature	[K]
T_C	Curie temperature	[K]
t_{dead}	Dead time	[s]
t_{fall}	Fall time	[s]
t_r	Retarded time	[s]
t_{rise}	Rise time	[s]
v	Speed of electromagnetic fields in a medium; voltage	[m/s]; [V]
V	Voltage; Potential; Volumetric object; Volume	[V]; [V]; [/]; $[\mathrm{m^3}]$

V_{clamp}	Voltage level to which the clamping circuit of this work limits the voltage during the transistor's off state	[V]
V_{diode}	Forward voltage drop across a diode	[V]
V_{ds}	Drain-to-source voltage of a transistor	[V]
V_{gs}	Gate-to-source voltage of a transistor	[V]
V_{GD}	Voltage, the gate-driver provides to turn the MOSFET on	[V]
V_{LS}	Voltage across the low-side transistor in a half-bridge	[V]
V_{out}	Output voltage	[V]
$[V_s]$	Vector containing the source voltages across the capacitive nodes in a PEEC-circuit	$[\mathrm{V}]_{(N\times 1)}$
v_{sat}	Saturated electron drift velocity	[m/s]
w	Width; Weighing function	[m]; [/]
W	Width; Length	[m]; [m]
X	Reactance	[Ω]
Y	Admittance	[S]
Z	Impedance	[Ω]
Z_0	Characteristic impedance of the vacuum	[Ω]
Z_c	Characteristic impedance of a transmission line	[Ω]
$\vec{\blacksquare}$	Vector ■	[dep.]
$[\blacksquare]$	Matrix ■	[dep.]
$\blacksquare'$	The quantity ■ referred to the primary side of a transformer	[dep.]
$\blacksquare_{avg}$	Average value of the quantity ■	[dep.]
$\blacksquare_{e}$	Effective value of the quantity ■	[dep.]
$\blacksquare^{e}$	Effective value of the quantity ■	[dep.]
$\blacksquare^{FHA}$	First harmonic of the quantity ■	[dep.]
$\blacksquare_{max}$	Maximum value of the quantity ■	[dep.]
$\blacksquare_{min}$	Minimum value of the quantity ■	[dep.]
$\blacksquare_{pp}$	peak-to-peak value of the quantity ■	[dep.]
$\blacksquare^{prim}$	Value of a quantity ■, referred to the primary side of a transformer	[dep.]
$\blacksquare^{sec}$	Value of a quantity ■, referred to the secondary side of a transformer	[dep.]
$\blacksquare_{rms}$	RMS-value of a quantity ■	[dep.]
$\blacksquare_{sp}$	Specific value of ■	[dep.]
$\widehat{\blacksquare}$	Amplitude of a quantity ■	[dep.]

$\blacksquare_\gamma$	with $\gamma = x$ or y or z or r or θ or ϕ or l: the corresponding component of quantity ■	[dep.]
$\blacksquare^T$	Transpose of a matrix quantity ■	[dep.]

Greek symbols:

δ	Duty ratio; Skin depth; Distance	[/]; [m]; [m]
ϵ	Permittivity; Linear dimensional scaling factor; Absolute error of voltage clamp device	[F/m]; [m]; [V]
ϵ_0	Vacuum permittivity	[F/m]
ϵ_r	Relative permittivity	[/]
ϕ	Phase difference between voltage and current; Magnetic flux; Scalar electric potential; Angle	[rad]; [Wb]; [J/C]; [rad]
γ	Ripple factor of a filter; Iteration variable; Propagation constant	[/]; [/]; [1/m]
λ	Thermal conductivity; Wavelength	[W/(m·K)]; [m]
μ	Permeability; Mobility of electrons or holes	[T·m/A]; [m^2/(V·s)]
μ_0	Vacuum permeability	[T·m/A]
μ_r	Relative permeability	[/]
ψ	Flux linkage	[Wb]
ρ	Specific resistivity; Volumetric charge density	[Ω·m]; [C/m^3]
σ	Electric conductivity; One of the bipolar coordinates; Surface charge density; Real part of the Laplace variable	[S/m]; [/]; [C/m^2]; [1/s]
τ	Time period; Time constant; One of the bipolar coordinates	[s]; [s]; [/]
ω	Pulsation	[1/s]

Contents

1 Introduction

1.1 Background

One of the aims of current research in power electronics is to increase the switching frequencies of the transistors. One of the reasons for this is that by increasing the switching frequencies, the power electronic circuits can be made smaller because the needed passive components can decrease in size. This is especially important in automotive and aerospace applications, where every cubic centimetre of space is worth a lot. Decreasing the size of power electronic circuits is also important in large server farms where each computer has a power supply and where thus different power supplies are present in a rack. Traditionally, the power supplies are cooled by fans or heat sinks and they all occupy a specific space. In these high-end applications, efficiency and space savings are very important. It is also possible to decrease the size of circuits by reducing the cooling requirements. If cooling becomes less critical, the size of the circuits is also reduced, because heat sinks and fans are less or no longer needed. Therefore, by increasing the efficiency of circuits, their size can also be diminished. This doctoral work does not investigate how to make the cooling requirements less strict, but looks at how to reduce the size of the passive components by increasing the switching frequencies in power electronic circuits. It asks the questions how to reach these high frequencies and secondly which problems arise at higher switching frequencies. It develops a method to quantitatively predict the deleterious effects due to the fast operation of switching components in a converter.

1.2 Aims of this thesis

This thesis aims to investigate:

- how to increase switching frequencies in power electronic converters,
- and what the potential problems are by doing this, for the converter itself and for its electromagnetic environment.

To the first topic, the next two Chapters will be dedicated, and to the second topic the subsequent two Chapters. Basically, in the next two Chapters, it will be investigated how power converters with increased switching frequencies can be built using soft-switching techniques or with hard-switching techniques. In the latter case, novel semiconductor devices must be employed, requiring a low amount of gate-charge. In the two Chapters dealing with the prediction of the problematic phenomena in fast power converters, numerical techniques will be developed to accurately calculate the distortion of the current and voltage waveforms in the presence of unwanted parasitics, and to calculate the electromagnetic fields that a fast-switching converter emits.

1.3 Chapter-by-chapter overview

This doctoral work first researches the possibilities to increase the switching frequencies in power electronic converters. Two different strategies are studied. In **Chapter 2**, it is examined how hard-switching converters can be operated at high switching frequencies. In order to operate transistors at a high frequency, it is important to keep the gate-charge as low as possible. This charge is needed to turn the transistors on or off. A gate-driver must deliver or consume this charge at every switching operation but can only deliver a limited current. Classical silicon components tend to be big and therefore have large parasitic input capacitances. They thus require a great amount of gate charge and their switching behaviour is slow. A novel semiconductor technology which is currently steadily advancing, tries to overcome these difficulties. It is the technology of wide-bandgap semiconductors. Because the gap between valence and conduction band is wide in these semiconductors, they are less prone to avalanche breakdown and can withstand a high inverse voltage as compared to silicon components with the same dimensions. In other words, the dimensions of the components can be reduced for the same blocking voltage. This means that semiconductor components can be made smaller and, therefore, their internal capacitances decrease in size and hence the components become faster. Gallium nitride is a promising wide-bandgap material. This work explains why gallium nitride is better for high-speed applications than silicon and quantifies also

the needed gate charge. For this research, a collaboration with Imec [Imec] was started. Imec developed a gallium nitride DHFET which is electrically characterized in this work from the point of view of a designer of power electronic circuits. Macroscopic quantities, important when designing power electronic circuits, such as the gate charge and the on-resistance, were measured and compared with those of traditional silicon components and also with those of the newer silicon superjunction MOSFETs. Since the switching frequency is only one aspect and efficiency is another -one can namely always increase the switching frequency, but this can lead to an unacceptable reduction of efficiency- attention was also paid to how efficient these components are in steady state. To this end, the dynamic on-resistance was measured. The measurements were accomplished with a novel voltage-clamping circuit. The dynamic on-resistance may be different from the static in HFETs, even at the same junction temperature, because of the current collapse phenomenon. The dynamic on-resistance is measured with an oscilloscope. The voltage-clamping circuit is designed to perform fast measurements and to overcome a low measurement resolution, which is associated with a straightforward measurement approach. In this Chapter of the work, the efficiency of the gallium nitride components of Imec is compared with that of commercial gallium nitride components produced by the company EPC, and with that of silicon components. For this purpose, a figure of merit is defined which takes both the conduction losses as well as the switching losses into account.

In a next part of the work (**Chapter 3**), a different strategy to realize high switching frequencies in power converters is studied: soft-switching. Soft-switching converters can operate according to several principles but in this work the class of the resonant converters is studied. Silicon components are used but the high switching frequencies are now achieved merely by intelligent switching strategies which are allowed by an appropriate converter topology. These resonant converters make use of coils and capacitors to excite resonances. The magnitude of the current in the resonant circuit must be large enough in order to discharge the output capacitors of the transistors before they switch on. Zero voltage switching is then obtained. If either the voltage or the current is zero when the switching occurs, there is no power dissipation and the switch has no switching losses. This zero voltage switching technique is used to increase the efficiency of a converter. Alternatively stated: the same efficiency can be obtained for an increased switching frequency. An increased switching frequency allows to decrease the size of the converter. An LLC-converter topology with a half-bridge is developed in this work. A literature review shows the state-of-the-art of the relationship between switching frequency and output power. Based on these data, a minimum frequency of 2 MHz and an output power of 50 W are selected for the converter of this work. This combination of power and frequency is with classical techniques not easy to reach. The conditions for zero voltage switching are carefully analyzed and this analysis is used to make a good choice for the MOSFETs which are to be used as switches in the converter.

A transformer is employed to create galvanic isolation and to transform the voltage to a lower level. Because the frequency is high enough, the parasitic elements of the transformer can be used as elements of the resonant circuit. In other words, no other external passive inductive components need to be employed to realize the inductive elements of the resonant circuit; only the transformer is used. This keeps the size of the circuit small. Optimal ratings for the components of the resonant circuit are determined by an exhaustive iteration analysis. The transformer is built with a ferrite core and a high-frequency model is devised which can be used in PSpice simulations. A fast gate-driver suitable to operate half-bridges is designed and built. It has the feature that the dead time can be controlled. The converter is first simulated and then constructed and the efficiency is determined. In this part of the work, it is demonstrated that resonant techniques allow to increase the switching frequencies while at the same time achieve acceptable efficiencies.

At higher switching frequencies, parasitics start to play a more prominent role, since parallel capacitances absorb more current and series inductances block more current. In addition, when fast switching components are used in converters, waveforms will be generated with steeper edges (higher dv/dt's and di/dt's). When those are applied to a circuit containing parasitics, the voltages and currents will begin to oscillate and exhibit overshoot, sometimes up to values of several times the steady-state value. These overvoltages and overcurrents stress the components heavily and can destroy them. Therefore, designers of power electronic circuits choose components with higher ratings than those which are necessary in circuits without parasitics. Also, the oscillating voltages and currents cause electromagnetic interference and can disturb the correct operation of electronics in their vicinity. Therefore, it is important that the oscillations that may arise due to the presence of parasitics in the circuits, can be modelled accurately. This work builds on a doctoral work presented in 2005 by ir. Bruno Bolsens at Electa [Bols 05]. In this work, use was made of the Method of Moments, to predict the effects of parasitics. In **Chapter 4** of this work, however, a different method is preferred: the Partial Element Equivalent Circuit (PEEC) method. This allows a circuit designer to think in terms of inductances, resistors, capacitors and voltage and current sources. An electromagnetic structure is modelled with an equivalent circuit consisting of the aforementioned components, and this circuit can then be connected to external components such as transistors, diodes, coils, capacitors, ... and can be solved with a Spice-like solver. The results are voltages, currents and powers, and not, as in the Moment Method, fields or potentials, of which it is much harder to get a feeling what they mean. The method of this work is implemented in Matlab. A freeware programme, PCBParC, is developed. It uses FastHenry and FastCap, also freeware software, designed to determine partial inductances and capacitances. There is both a quasi-static version and a full-wave version of PCBParC and these were tested on linear and non-linear circuits. It can be concluded that parasitics have many undesirable effects in converters employing

rapid switches and that the modelling of these parasitics cannot be neglected.

In the previous Paragraph, it was elaborated that due to the fact that high-speed components are used at high switching frequencies and due to the presence of parasitics, the voltages and currents in a converter exhibit an oscillating behaviour. These rapid variations of charges and currents are sources of electromagnetic fields. They can disturb other electronics in the vicinity and it is useful if the magnitude and influence of these fields can be predicted. Therefore, this work is extended in **Chapter 5** with a technique to calculate electromagnetic fields. A full-wave method is outlined, which is used in combination with the method of the previous Chapter, the PEEC-technique. This technique calculates the currents through and the potentials on the PCB-traces of power electronic converters. Then, the method of this Chapter calculates the electromagnetic fields due to these currents and potentials. The method has both a frequency-domain expression and a time-domain expression. The formulas are referred to as the 'Jefimenko equations' in the latter case. The method is implemented in Matlab and verified by comparing with the analytically known fields around a two-wire transmission line carrying a DC-current, and with the fields around a Yagi-antenna and around a dipole antenna. Thereafter, the method is applied to switching converters. There is very little literature where a full description of the dimensions of the converter structure is given, together with a good description of the electromagnetic fields. Therefore, it was decided to apply the method of this work to the case described in the doctoral work of Bolsens and compare both results. Bolsens simulated a buck converter with the Moment Method. His results for the radiated power do quantitatively not match well with the results produced by the method of this work. However, the conclusion that around power electronic converters a high-frequency-channel is present between the switch and diode, due to which part of the converter's radiation losses are produced, could also be drawn. The near fields of the buck converter are then calculated with the method of this work on a plane, which is only a few millimetres above the PCB. The near fields are compared with the results obtained with a commercial field calculation software programme (Comsol), which uses the Finite Elements technique. However, the calculation time of the method of this work is much smaller than that of Comsol. The method is also applied to the reversed buck converter of the previous Chapter in order to show how the method may be applied to predict the results of EMC-compliance tests.

Chapter 6 finally concludes this work. It summarizes the problems encountered in this work, it summarizes the important lessons learned, and gives advice for future work.

1.4 Professional collaborations

The author wishes to thank Imec, and in particular Jo Das, Marianne Germain, Steve Stoffels and Kai Cheng, for the fruitful collaboration regarding the transistor characterization work. Also, he likes to express his gratitude to his colleagues from Electa, Ratmir Gelagaev and Jordi Everts, for helping with the measurements of Chapter 2, and to Jeroen Van den Keybus of Triphase N.V., for the discussions leading to the development of the voltage-clamping circuit for measuring the dynamic on-resistance of transistors. Also Bruno Bolsens of Snox Automation BVBA, deserves a special mentioning, for discussing the results of the calculation of the electromagnetic fields. The author offers his thanks furthermore to Peter Tant of Triphase N.V., for helping with the development of the fast gate-drivers, and to Jeroen Zwysen of Electa, for using his Moment Method software tool and helping with the field calculations. Kristof Engelen deserves a special mentioning for the many enlightening discussions and valuable contributions, for instance the solution of the problem of Section 5.4. The author thanks moreover Prof. Elias Jarlebring of KTH, Stockholm for the insight provided by him in the stability analysis of delay differential equations. The author thanks also Prof. Davy Pissoort of KHBO, and finally Prof. Ruth Vazquez Sabariego of Electa for her help with Gmsh and GetDP and with the reading of the text.

1.5 Personal contributions

The most important novel contributions of this work are:

- The development of a voltage-clamping circuit for accurately measuring the dynamic on-resistance of a MOSFET or HEMT.
- A complete description of all the steps in the design of a resonant LLC-converter, being the first soft-switched converter, realized in research group Electa.
- A method to determine the optimum values of the resonant tank elements.
- The development of an accurate high-frequency model for a transformer.
- The analysis of the necessary and sufficient conditions for zero voltage switching.
- The development of a freeware PEEC software programme, which can generate quasi-static and full-wave models of PCB-tracks and extracts a Spice-netlist.

- The development of the method for calculating electromagnetic fields around a power converter, as outlined in Chapter 5, which is based on Jefimenko's equations and which is fast and able to calculate the fields in both the time- and the frequency-domain.

2

Application of Wide-Bandgap Semiconductors in Fast Power Electronics

2.1 Introduction: wide-bandgap semiconductors: material properties and advantages over silicon

2.1.1 Material properties

Recently, wide-bandgap (WBG) semiconductors are more and more being utilized for power devices used in switching applications. Much research is being invested in developing silicon carbide (SiC), gallium nitride (GaN) and diamond semiconductors, which are examples of wide-bandgap semiconductors.

A wide-bandgap semiconductor is a material having a bandgap larger than 2 eV [Taka 07], being almost twice as large as that of silicon (1.12 eV [Ozpi 03] [Taka 07]). Silicon carbide and gallium nitride offer bandgaps of 3.03 eV (for 6H-SiC), 3.26 eV (for 4H-SiC) and 3.45 eV (for GaN) [Ozpi 03] [Taka 07]. Some important physical characteristics of the most important wide-bandgap semiconductors are shown in Table 2.1 and are compared with the properties of silicon and gallium arsenide [Ozpi 03] [Boey 06].

Table 2.1: Physical characteristics of silicon, gallium arsenide and comparison with some important wide-bandgap semiconductors.

Property	**Si**	**GaAs**	**6H-SiC**	**4H-SiC**	**GaN**	**Diamond**
Bandgap E_g [eV]	1.12	1.43	3.03	3.26	3.45	5.45
Relative permittivity ϵ_r [/]	11.9	13.1	9.66	10.1	9	5.5
Electric breakdown field E_c [kV/cm]	300	400	2400	2000	3300	10000
Electron mobility μ_n [cm^2/(Vs)]	1350	8500	370	700	900	2200
Hole mobility μ_p [cm^2/(Vs)]	600	400	101	115	850	850
Thermal conductivity λ [W/(cm.K)]	1.5	0.46	4.9	4.9	1.3	22
Electron saturation drift velocity v_{sat} [$\times 10^7$ cm/s]	1	1	2	2	2.2	2.7

2.1.2 Advantages of WBG materials

A wide bandgap has several advantages. Because of the greater bandgap, wide-bandgap materials can withstand a greater reverse voltage for the same thickness in comparison with silicon ([Moha 02], section 19.5 Avalanche Breakdown). Hence, for the same voltage rating, devices can be made smaller. Therefore, the length of the channel, the chip area and therefore also the gate-to-drain capacitance in vertical Field Effect Transistors (FETs) decrease. This, and the fact that the saturation drift velocity is more than twice than that of silicon (Table 2.1), results in faster switching behaviour for the wide-bandgap devices.

Moreover, because of the higher breakdown field strength than silicon, the on-resistance of diodes and transistors decreases [Bali 08], for the same dimensions of the component. Fig. 2.1 shows the static specific on-resistance of diodes and transistors for different materials. The relationship is derived using expressions from [Bali 08], [Baik 04], [Zegh 09] and [Hanm 05] (section 2.1.1). The line representing this relationship for silicon MOSFETs is called the *Silicon Limit*. Also for silicon Super-Junction (SJ) MOSFETs the relationship between specific

on-resistance and breakdown voltage is shown [Fuji 97]. It is a linear relationship. It can be seen that the resistance of silicon devices is about two orders of magnitude worse than that of SiC-devices, that there is also a difference between the on-resistance of 4H- and 6H-SiC-devices and that devices fabricated from 2H-GaN can have an on-resistance which is a factor 9.5 smaller than devices made from 4H-SiC. Some points are plotted, indicated by the letters A to K, denoting recently developed AlGaN/GaN HEMTs. The corresponding reference to the article in which these devices were announced is given in Table 2.2.

Table 2.2: AlGaN/GaN HEMTs, used in Fig. 2.1.

Letter	**Reference**	**Letter**	**Reference**
A	[Iked 10]	B	[Sait 10a]
C	[Xing 04]	D	[Zhan 01]
E	[Zhan 02]	F	[Sait 10b]
G	[Dora 06]	H	[Uemo 07]
I	[Baha 10]	J	[Iked 08]
K	[Tipi 06]		

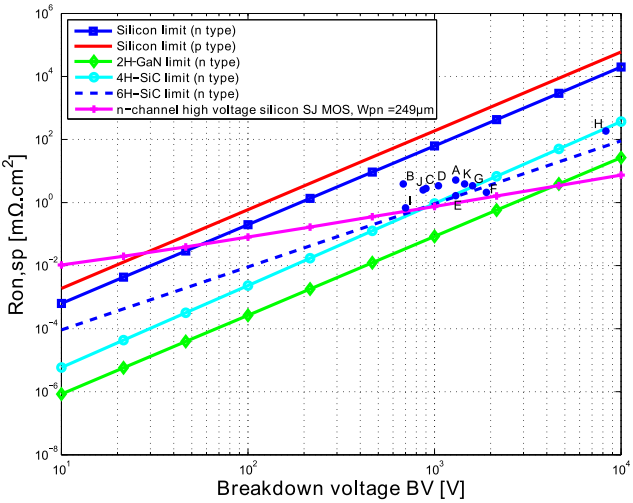


Figure 2.1: Specific on-resistance versus breakdown voltage: material limits and performance of recently developed devices.

Not only the capacitances and on-resistance of wide-bandgap semiconductor devices are smaller than those of silicon devices, also, a wide bandgap implies a lower intrinsic carrier density n_i than in silicon at the same temperature, because [Zegh 09]:

$$n_i = \sqrt{N_c N_v} e^{-E_g/(2kT)} \tag{2.1}$$

with T the temperature [K], k Boltzmann's constant [J/K], E_g the bandgap [J] and N_c and N_v the effective density-of-states in respectively the conduction band and the valence band [$m^{-3}J^{-1}$]. Furthermore, the leakage current in a reversely biased pn-junction is given by [Neud 02]:

$$I \approx -qAn_i \left[\frac{n_i}{N_D} \sqrt{\frac{D_P}{\tau}} + \frac{W}{2\tau} \right] \tag{2.2}$$

where q is the elementary charge [C], A is the area of the pn-junction, W is the width of the junction depletion region, N_D is the n-type doping density [m^{-3}] , D_P is the hole diffusion constant [m^2/s] and τ is the minority charge carrier lifetime [s]. A lower intrinsic carrier concentration at a specific temperature therefore means that wide-bandgap transistors and diodes can operate at higher temperatures than silicon devices. It has been shown [Neud 02] that GaN transistors can operate up to 300 °C, and even [Medj 06] up to 1000 °C in vacuum. Silicon devices on the other hand, stop working properly at 140-150 °C [Neud 02] [East 02]. Also, SiC devices have been demonstrated to work well at temperatures in the 300-600 °C-range [Brow 97] [Neud 00]. Furthermore, because the thermal conductivity of the wide-bandgap devices is higher than silicon, cooling them is easier [Taka 07].

The focus of this work lies on the switching characteristics of power semiconductor devices. A higher switching frequency is advantageous for several reasons [Fins]:

- It enables a faster transient response in power converters.
- A higher switching frequency reduces the requirements of passive components in converters. In general, the inductances and capacitances in energy-storage circuits or filtering circuits in power converters are inversely proportional to the switching frequency and are directly proportional to their volume. Therefore, an increased frequency implies a smaller converter.
- At sufficiently high frequencies, batch fabrication may become possible, enabling higher levels of integration.

However, as will be shown in this work, waveforms in power converters with a higher frequency content are subjected to many problems, such as problems with signal integrity, with increased ringing, with increased overshoot of voltages and currents causing a greater electrical stress to power devices and even with unwanted electromagnetic radiation. Because of the many advantages of wide-bandgap semiconductors, the author of this work believes that, if wide-bandgap power components can be fabricated at a low cost and with a good quality, they will replace the classic silicon devices in many applications in due time. If they

are used, they will be operated at higher switching frequencies and with lower rise- and fall-times than is the case today, with all the deleterious effects that are mentioned before. Therefore, researching the design of power converters which are subjected to high frequencies, is necessary. This is the motivation for undertaking this work.

2.1.3 Figures of merit

In order to quantify "how good" the wide-bandgap semiconductor materials are in comparison with silicon, performance indices, known as the *figures of merit*, were devised. They compare the different wide-bandgap materials with each other and with silicon, for different applications. Baliga's figure of merit, $BFOM$ [Bali 10], allows to compare the static on-resistance of devices fabricated from different materials. For the same geometry, the on-resistance is inversely proportional to:

$$BFOM = \epsilon \mu_n E_c^3 \tag{2.3}$$

with ϵ the permittivity, μ_n the electron mobility and E_c the electric breakdown field. $BFOM$ is therefore a measure for the conduction losses in power semiconductors.

Furthermore, there exists a second figure of merit, attributed to Baliga, which is a high-frequency figure of merit. It is denoted by $BHFFOM$. It is inversely proportional to the square root of the sum of the switching losses and conduction losses in MOSFETs. It is given by (cf. [Wang 07], formula (2-10)):

$$BHFFOM = \frac{1}{R_{on,stat,sp} Q_{g,sw,sp}} \tag{2.4}$$

with $R_{on,stat,sp}$ the specific static on-resistance and $Q_{g,sw,sp}$ the specific gate charge. Reference [Bali 89] shows it is also equal to:

$$BHFFOM = \frac{\mu_n E_c^2}{2} \sqrt{\frac{V_{GD}}{(BV)^3}} \tag{2.5}$$

with BV the breakdown voltage and V_{GD} the voltage which the gate-driver applies to the devices to turn them on.

Thirdly, there is Johnson's figure of merit, $JFOM$, which is proportional to the power-frequency product of low-voltage transistors [John 65]:

$$JFOM = \left(\frac{E_c v_{sat}}{2\pi} \right)^2 \tag{2.6}$$

with E_c the critical breakdown electric field and v_{sat} the saturation drift velocity. This implies that for a specific material, the relationship between power and frequency is hyperbolic for low-voltage transistors.

Finally, the Keyes's figure of merit, $KFOM$, provides a thermal limitation to the switching behaviour of transistors [Keye 72]:

$$KFOM = \lambda \sqrt{\frac{c v_{sat}}{4\pi\epsilon_r}} \tag{2.7}$$

with λ the thermal conductivity, c the speed of light and ϵ_r the relative permittivity.

For a few semiconductors, these figures of merit are calculated with the data of Table 2.1 and their values, relative to the values for silicon, are shown in Table 2.3.

Table 2.3: Comparison of important figures of merit for some semiconductors, relative to those for silicon.

FOM	**Si**	**GaAs**	**6H-SiC**	**4H-SiC**	**GaN**	**Diamond**
BFOM	1	16.4	114	130	671	27896
BHFFOM	1	11.2	18	23	81	1811
JFOM	1	1.8	256	178	586	8100
KFOM	1	0.29	5.1	5	1.48	35.5

2.1.4 Where is it advantageous to use wide-bandgap power devices?

High frequency power electronic circuits are especially advantageous to use from the perspective of miniaturization. Higher switching frequencies allow to make the passive components surrounding the power switches smaller. Space-saving is in many applications important, but certainly in the automobile and the aerospace industry.

Also, the property of wide-bandgap semiconductors to operate at higher temperatures is an extra advantage in the extreme conditions these devices are sometimes subjected to. For instance, in the oil and gas industry or the geothermal drilling industry, where electronics for telemetry are developed, wide-bandgap semiconductors benefit greatly from their capabilities to withstand high temperatures.

Decreasing the size of the required electronic circuits is certainly an advantage in the electronic ballasts that ignite lamps. High Intensity Discharge lamps are ignited at 300 kHz by a voltage produced by an H-bridge delivering a square wave voltage that is being filtered by an LC-tank [Tant 10]. Augmenting the frequency allows to decrease the size of this LC-tank, provided that the lamp

still ignites at these higher frequencies. Manufacturers of lamp ballasts benefit thus from the wide-bandgap power semiconductors.

Also manufacturers of motor drives profit from smaller electronics, higher efficiencies and higher reliabilities.

Advantages due to miniaturization can also be of great interest in high power applications such as in the electric heating industry and in the field of energy transmission and distribution where Flexible AC Transmission Systems (FACTS) and active filters are used.

The higher attainable powers, the smaller components, the reduction of harmonic pollution, the higher efficiencies and the possibility to integrate the semiconductors in a hot environment, are great advantages of wide-bandgap semiconductors for aforementioned application areas. The same advantages also facilitate the proliferation of renewable energy sources and distributed generation.

2.2 Characterization of wide-bandgap transistors

2.2.1 Collaboration with Imec

In 2008, the micro- and nanoelectronics research institute Imec [Imec] asked research group Electa [Elec] to utilize their newly developed GaN power transistors [Das 11] in actual power converters in order to see how these components behave in real-life test conditions. Furthermore, Imec wanted to know which device parameters are important for power electronic design engineers and started a collaboration with Electa for determining and measuring these electrical characteristics. Electa agreed to this collaboration because it researches, among other topics, how power converters behave and how they should be controlled at high switching frequencies, and wide-bandgap semiconductors provide the advantage of exploiting these increased frequencies.

Imec's second generation devices are normally-off (enhancement-mode) lateral Double-Heterostructure Field Effect Transistors (DHFETs). The width of the gate is 57.6 mm and its length is 1.5 μm. They are fabricated starting from a $Si_3N_4/Al_{45}Ga_{55}N/GaN/Al_{18}Ga_{82}N$ MOCVD grown heterostructure on a $Si < 111 >$ substrate. The different devices on the substrate are then isolated from each other, ohmic contacts are made and the gate is fabricated. It is composed of different gate-fingers. Next, the surface is passivated with Si_3N_4 and lastly, an interconnection layer is deposited. Finally, the dies are packaged on an AlN ceramic carrier layer, acting as a heat spreader. Also other types of devices which are normally-on (depletion-mode) needed to be characterized in this work. In order to obtain a device with a threshold voltage which is still

negative but closer to zero, the $Al_{45}Ga_{55}N$ barrier thickness is scaled down to 5 nm and at the same time, the in-situ grown Si_3N_4 is selectively removed under the gate.

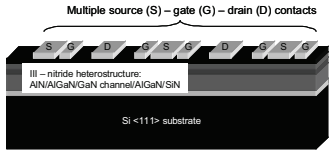


Figure 2.2: Cross-section of Imec's GaN DHFET device.

2.2.2 Design and construction of a reversed buck converter

In order to test Imec's GaN devices in real-life conditions, a reversed buck converter was built (Fig. 2.3), in collaboration with Ratmir Gelagaev from Electa. The reversed buck converter of this work is designed for a maximum input or output power of 8 kW, with a voltage of 400 V and a current of 20 A. The coil is designed for a minimum switching frequency of 150 kHz and a maximum frequency of 1 MHz. The transistor's source is connected to the ground, hence the name 'reversed' buck. This type of topology is chosen instead of a normal buck topology because it allows to use a gate-driver which is not isolated.

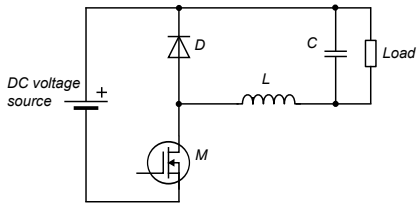


Figure 2.3: Basic topology of a reversed buck converter.

If possible, transistors with TO-247-packages are chosen because these have a large package size thus allowing good heat transfer to a heat sink. Cooling occurs with a heat sink (0.33 K/W, 97CN-02500-A-200 - HS Marston) and natural convection. Between the semiconductor package and the heat sink, there is a heat spreader made from an alloy of copper and beryllium, having a thickness of 8 mm. The PCB-traces are about 12 mm wide and have a thickness of 70 μm. When a current of 20 A flows through these traces on an FR4-substrate, they heat up 30 °C above the ambient temperature [Ferr]. The diode is an Infineon silicon carbide Schottky diode (IDT16S60C (16 A, 600 V)), in a TO-220 package.

The minimally necessary inductance value of the coil is designed for the lowest switching frequency ($f_s = 150$ kHz), the highest input voltage ($V_{in} = 400\ V$), the worst case duty cycle ($\delta = 2/3$) and for the maximum output power ($P_{out} = 8$ kW). The minimum inductance, necessary for a 10 % peak-to-peak current ripple, is [Moha 02]:

$$L_{min} = V_{in}^2 \left(\frac{2}{3}\right)^2 \left(\frac{1}{3}\right) \frac{1}{f_s(0.1P_{out})} = 198\ \mu\text{H} \tag{2.8}$$

The absolute and relative ripples on the inductor current in function of the duty ratio, are given for continuous conduction mode (CCM) by [Moha 02] (Fig. 2.4a, 2.4b, 2.4c):

$$\Delta i_{L,pp} = V_{in}\delta(1-\delta)\frac{1}{f_s L} \tag{2.9}$$

$$\frac{\Delta i_{L,pp}}{I_{out}} = V_{in}^2\delta^2(1-\delta)\frac{1}{f_s P_{out}} \tag{2.10}$$

The minimum value of the output capacitance for an output voltage ripple of 5 %, is given by [Moha 02]:

$$C_{min} = \frac{1}{8f_s^2}\frac{1}{0.05L_{min}} = 56.3\ \mu\text{F} \tag{2.11}$$

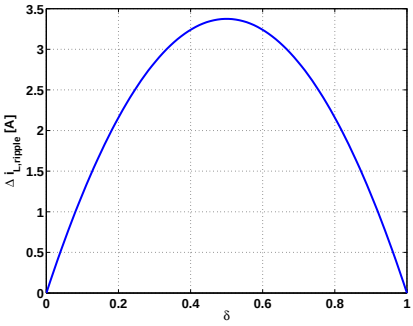
With the values of $L = L_{min}$ and $C = C_{min}$, the LC-output filter has a cutoff frequency of:

$$f_c = \frac{1}{2\pi\sqrt{L_{min}C_{min}}} = 15.1\ \text{kHz} \tag{2.12}$$

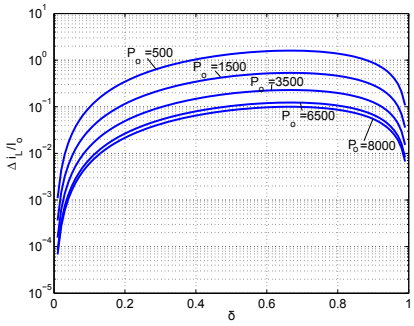
which is much smaller (a factor of 10) than the switching frequency of 150 kHz. Therefore, the filter is able to attenuate the fundamental and the harmonics of the switching frequency well.

The coil is designed with the procedure of [Boss 05], chapter 2. An EPCOS PM74/59 core is chosen, fabricated from the ferrite material N87. The coil has 14 windings and an air gap of 1.3 mm. The measured inductance is 220 μH. Litz wire is used (Pack Feindrähte, Rupalit V 155) where each of the 50 strands has a diameter of 0.15 mm (the skin depth in Copper at 150 kHz is 0.2 mm, but it is 0.076 mm at 1 MHz). The outer diameter of a single wire is 1.8 mm; three wires in parallel are used to carry a total current of 20 A.

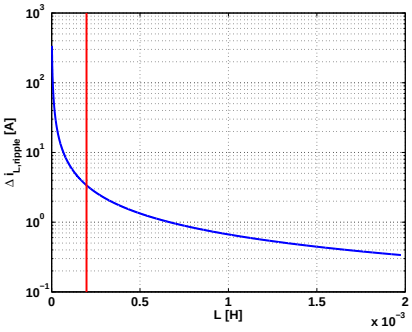
Two output capacitors in parallel are used (2x470 μF, 450 V, electrolytic capacitors, Panasonic EEUED2W470). The same type is used at the input: two similar electrolytic capacitors are there used in parallel, and furthermore a ceramic 1 μF, 630 V capacitor is also placed as close to the diode and transistor as possible. The total size of the PCB is 23.3 cm x 10.4 cm. A test setup is made with 3 in series connected DC power supplies (Delta Elektronica SM 120-13),



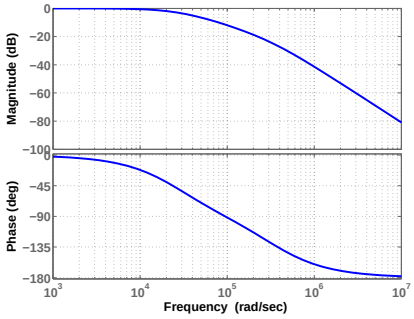
(a) Peak-to-peak ripple on the inductor current versus duty ratio with $L = L_{min}$ for CCM.



(b) Fractional peak-to-peak ripple on the inductor current versus duty ratio with $L = L_{min}$ for CCM.



(c) Peak-to-peak ripple on the inductor current versus inductance for the worst case duty ratio ($\delta = 1/2$) and for CCM.



(d) Bode diagram of the output LC-filter with $L = L_{min}$ and $C = C_{min}$.

Figure 2.4: Choosing the inductance and capacitance values in the reversed buck-converter.

providing a voltage which can be regulated between 0 and 327 V and which can deliver a current up to 13 A. At the output side, two types of potentiometers can be placed: $0 - 90\ \Omega$, 15 A or $0 - 300\ \Omega$, 9 A.

A picture of the converter is shown in Fig. 2.5. As can be seen, there is a little window in the PCB so that a thermal camera can be placed for capturing the temperature distribution around the transistor.

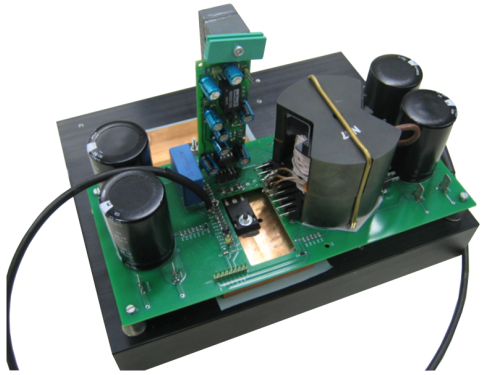


Figure 2.5: Picture of the designed and constructed reversed buck converter.

2.2.3 Design and construction of a gate-driver

A fast, dedicated gate-drive circuitry for driving the DHFETs, introduced in previous Section, is built for the reversed buck converter, which is used for measuring important electrical characteristics of the semiconductor devices. Although this kind of converter does not require electrical isolation in the gate-driver, it is desirable to design a circuit which does possess this characteristic, in order to be able to make use of it in converters where this capability is necessary. The gate-driver is built in collaboration with Peter Tant and Ratmir Gelagaev from Electa.

One of the shortcomings in the existing literature about gate-drivers is that it is often not mentioned how the electrical isolation of the gate-driver is realized. Neither is it clear how the high and low level of the gate-to-source voltage are generated. Furthermore, some of the GaN-devices of concern are 'normally-on' transistors, as it is also the case for many other experimental devices. Therefore, the driver needs to be robust and has to switch off the device immediately by applying a negative gate-to-source voltage if the driver fails. Also, experimental GaN-transistors are constantly under development and it has to be possible to change the levels of the applied gate-to-source voltage. The reason for this is that when a new transistor is developed which requires other gate-to-source voltage levels, the same driver can be used, but only small changes have to be made to the components of the driver. Finally, another requirement for the driver is that it must be possible to construct it with readily available electronic components.

A gate-driver which is fast, isolated and robust, which has easily adjustable voltage levels and which is constructed from readily available electronic components, is developed in [Jacq 10]. Further details about the implementation can be found in that article, but the gate-driver's topology will also be briefly

outlined here.

The topology of the gate-driver is presented in Fig. 2.6. In the centre of the circuit, there is an isolated DC-DC-power converter. Because of the requirement that standard, readily available electronic components have to be applied, the NMH0515DC-converter is used. This converter transforms the 5 V input voltage into -15 V and +15 V having a common 0 V-ground. This 0 V-ground is connected to the source of the transistor to be driven. The gate driver is fed by an external 5 V DC voltage supply and the input signal, determining the frequency of the driver, is a block pulse of amplitude 5 V, generated by a pulse generator. There are two galvanic isolations in the gate driver: one in the NMH0515DC-voltage converter and the second in the digital isolator ADUM1200CRZ. The latter galvanically isolates its input from its output, but input and output voltages are basically the same; there is only a small delay between the two. After the digital isolator, the voltage signal may contain some noise. This noise can be reduced by a Schmitt-trigger (SN74LVC1G17DBVR).

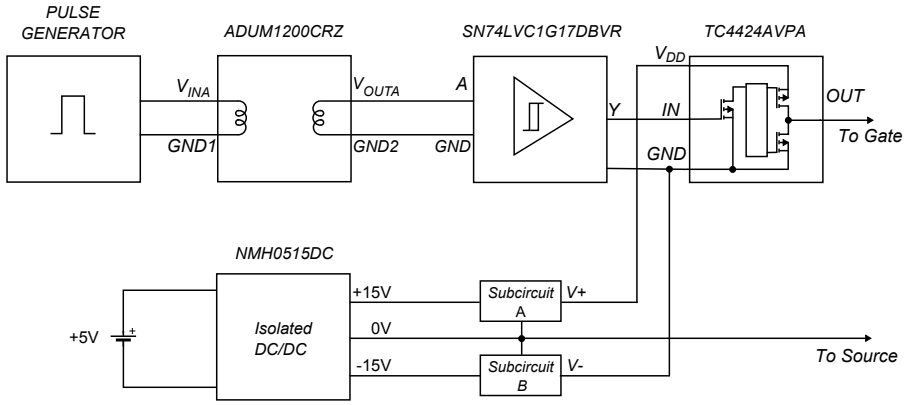
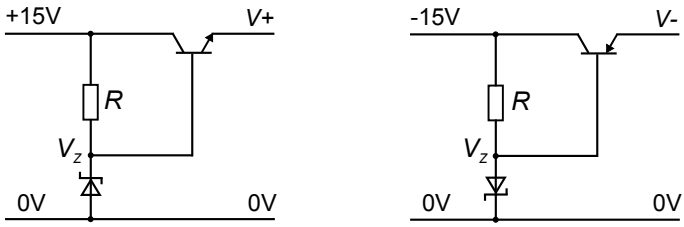


Figure 2.6: Schematic of the basic principle of the gate-driver.

The driver can generate a positive (or zero) gate-to-source voltage for switching the transistor on and a negative (or zero) voltage for switching it off. The values of both voltages can be adjusted by using appropriate components in the two subcircuits A and B, each containing emitter-follower circuits. The subcircuit A is shown in detail in Fig. 2.7a. It converts the +15 V from the DC/DC-converter to a lower positive voltage which is determined by the Zener diode voltage V_Z. One can also use light-emitting diodes (LEDs) instead of the Zener diodes. In that case, the LEDs are reversely connected with respect to the direction of the Zener diodes in the Figure.

The proposed driver can easily be extended to a resonant version by putting a resonant tank-circuit between the gate of the transistor and the TC4424A.



(a) Emitter-follower A.

(b) Emitter-follower B.

Figure 2.7: npn- and pnp-emitter-followers.

However, even using the conventional driver design, a frequency of multiple megahertz can be reached.

2.3 Measurements

In this Section, some measurements will be discussed in order to determine the characteristics of GaN-semiconductor devices, which are important for power electronics engineers designing converters. The GaN-devices which are examined are the Efficient Power Conversion Corporation (EPC) [EPCc] EPC1010 and Imec's first and second generation GaN-HFETs. Their characteristics are compared with those of the SPW52N50C3 silicon Coolmos, developed by Infineon [Infi]. The measurements are performed in collaboration with Ratmir Gelagaev and Jordi Everts, from Electa.

2.3.1 Static on-resistance in function of drain current

Methodology

A gate-driver provides a voltage pulse between the gate and source of the device-under-test, long enough to let the current and on-resistance reach steady state but short enough not to heat the device too much. If data about the thermal impedance of the device is known, a maximum on-time can be determined. The temperature has an important influence on the static on-resistance $R_{on,stat}$; therefore, in measuring $R_{on,stat}$, the ambient temperature must be specified and it must be made sure that the current does not heat up the transistor.

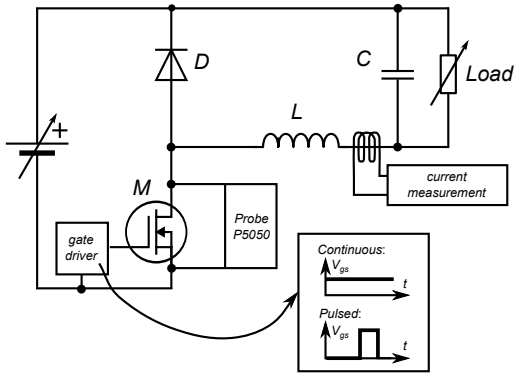


Figure 2.8: Measuring the static on-resistance versus the drain current.

The output capacitors of the reversed buck power circuit must ideally be removed, in order to avoid too large inrush currents, but even when they are present the buck's coil represents a sufficiently large impedance limiting the inrush current. The time constant of the current is, without the output capacitors, L/R with L the inductance of the buck's coil and R the load resistance. Also, the gate voltage determines the on-resistance and must be specified in the measurement results. The gate-to-source voltage is kept constant here for every device. The voltage across the device and the current through it are measured with respectively a Tektronix P5050 probe and a LEM PR50 current clamp probe. The division of the two yields the static on-resistance. It must be noted that at each measurement, the voltage probes must also be short-circuited and

the current probes must be closed but must enclose no wires. The voltages and currents that are measured in these cases, represent an offset which must be subtracted from the actual measurements. The measurement method is depicted in Fig. 2.8.

$R_{on,stat}$ in function of I_{ds}

The Coolmos and the EPC-device are turned on for 30 ms. For the Coolmos, the thermal impedance between junction and case is then 0.3 K/W. At 10 A, and with an on-resistance of 70 mΩ, as found in the datasheet, the loss is 0.7 W and the junction heats 0.21 K above the casing temperature. It is thus be found that this pulse does not heat the transistor very much.

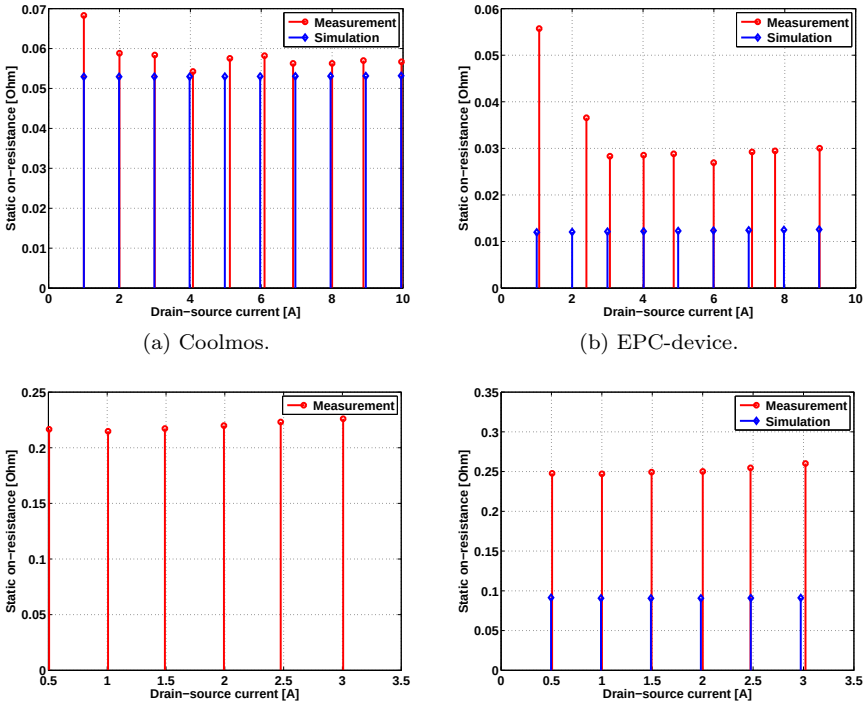
Unfortunately, due to a low availablity of Imec's components, no pulsed measurement for determining the static on-resistances were performed for Imec's devices. However, the static on-resistance was determined when they were continuously on, thus heating up and giving not so reliable values for the resistance.

For the Coolmos, the EPC-device and Imec's second generation transistor, the on-resistance is determined by measurement and also by simulation in PSpice and both are compared (Fig. 2.9a-2.9d). For Imec's first generation transistor, no simulation model was available and a comparison with simulation results could not be given. The gate-to-source voltage and ambient temperature is given in Table 2.4.

From the Figure, it can be seen that Imec's and EPC's simulation models are greatly optimistic about the on-resistance as compared to the results that were obtained in the measurements. Furthermore, it can be seen that for the lower currents, the on-resistance is higher than for higher currents. However, quickly, the resistance reaches a steady value.

Table 2.4: Gate-to-source voltage and ambient temperature for the experiment determining the static on-resistance as a function of the drain current.

	V_{gs} [V]	T_a [degrees Celsius]
Coolmos	15.84	24
EPC	4.9	25
Imec 1st gen.	0.4394	25.7
Imec 2nd gen.	0.6155	27



(a) Coolmos.

(b) EPC-device.

(c) Imec's first generation device.

(d) Imec's second generation device.

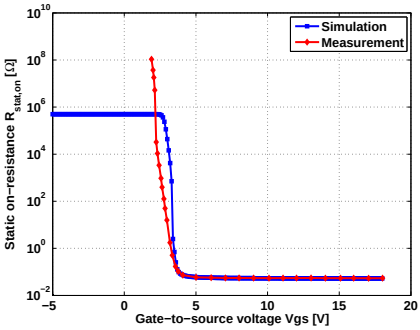
Figure 2.9: Static on-resistance versus the drain current.

$R_{on,stat}$ in function of V_{gs}

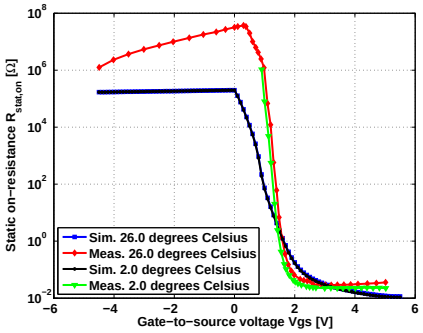
Because the gate-to-source voltage influences the static on-resistance a lot, this dependency is examined. The gate voltage is applied and the on-resistance is measured with a Keithly 2000 high precision multimeter. A comparison with PSpice simulation data is given (Fig. 2.10a-2.10d). No data are available for Imec's first generation devices, and for the second generation devices only the simulation results (at 25 degrees Celsius) are given. The on-resistance of the EPC-component is measured and simulated in function of the gate voltage for two ambient temperatures, 2 and 26 degrees Celsius. Also the temperature coefficient α of the static on-resistance of the EPC-device, defined in the relationship $R = R_0(1 + \alpha(T - T_0))$, is depicted. The simulations and measurements of the resistance of the Coolmos are done at 23.7 °C.

In order to obtain the temperature of 2 degrees Celsius, the EPC-device is submerged in deionized and demineralized water, being in thermal equilibrium with water containing melting ice cubes. An electrically isolating bag separates

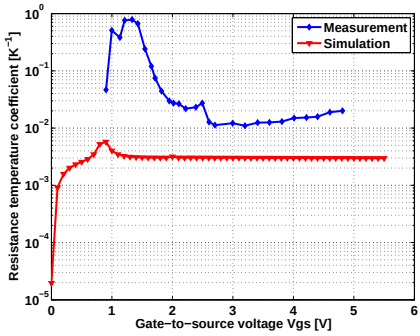
the two fluids from each other. The deionized and demineralized water has a resistivity of 10 MΩ/cm. In order to further protect the device against the water, it is covered with a thin layer of low hygroscopic Stycast 1090 epoxy resin.



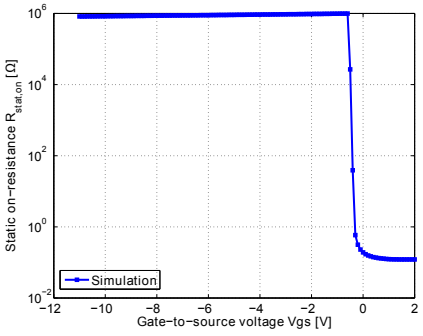
(a) Static on-resistance versus gate-to-source voltage for the Coolmos.



(b) Static on-resistance versus gate-to-source voltage for the EPC-device.



(c) Temperature coefficient of the on-resistance of the EPC-component versus gate-to-source voltage.



(d) Static on-resistance versus gate-to-source voltage for Imec's second generation device.

Figure 2.10: Static on-resistance and its temperature coefficient versus gate-to-source voltage.

2.3.2 Dynamic on-resistance

Methodology

The on-resistance that occurs after applying high-voltage swings to the drain terminal of the semiconductor switching device, is further referred to as the dynamic on-resistance $R_{on,dyn}$. The dynamic on-resistance of a transistor is

measured in switching mode based on Ohm's law:

$$R_{on,dyn} = \left.\frac{V_{ds}}{I_{ds}}\right|_{on} \tag{2.13}$$

Recently developed high voltage semiconductor switching devices frequently perform high speed switching operations and the static on-resistance calculated from direct-current measurements is not sufficient as a guideline to predict the conduction losses. The reason for this is that the on-resistance is determined by the junction temperature which is unknown. Also, heterostructure wide-bandgap semiconductor transistors are subject to a phenomenon known as *current collapse*, also called *charge trapping* [Vetu 01][Mene 04][Ever 10][Jin 13]. This causes the on-resistance to be dependent on the voltage the transistor has to withstand during its off-state.

The measurement of the dynamic on-resistance involves however difficulties. During switching operation, the high voltage and low current state (the off-state) repeatedly alternates with the low voltage and high current state (the on-state). The measurement of the dynamic on-resistance is typically performed by observing waveforms using an oscilloscope to allow changes in time to be followed. In measurements of voltage waveforms, if the range of the oscilloscope is not set wide enough to measure both on-state and off-state voltage levels, the characteristics of an amplifier inside the oscilloscope are distorted, due to a phenomenon known as "Oscilloscope Overdrive" and the lack of recovery thereof ([Dobk 11], Chapter 24), resulting in failure to accurately measure the on-state voltage. Therefore, the measurement scale of the oscilloscope has to be set in a range wide enough for the high voltage (off-state) and low voltage (on-state) to be followed. This, however, reduces the accuracy of the low voltage measurement, which is necessary for the measurement of the dynamic on-resistance. Typical oscilloscopes have an 8-bit A-D-converter providing a measurement resolution of 256 levels. In a case where the off-state voltage is e.g. 300 V the measurement resolution becomes 300 V/256 = 1.17 V resulting in a completely unreliable measurement. The new GaN-HEMTs exhibit a lower dynamic on-resistance and a higher switching speed than the conventional silicon power MOSFETs, requiring an even higher resolution.

Conventional circuits partially solve this problem by clamping the off-state voltage to a lower value. However, they introduce problems such as voltage peaks and measurement delays due to *RC*-time constants. These problems become worse with an increasing switching frequency and decreasing switching times resulting in failure to accurately measure the voltage waveforms.

To address these problems, a novel voltage clamping circuit is proposed which improves the accuracy of the on-state voltage waveform measurement. Unlike traditional circuits, the presented voltage clamp circuit does not introduce

delays caused by RC-time constants keeping the voltage waveform clear even during state transitions of the semiconductor switching device. The presented voltage clamp circuit performs well for frequencies up to 1 MHz.

Two conventional circuits, also using the voltage clamping principle, are first explained and discussed to illustrate their disadvantages.

The on-state current measurement is not discussed here as it can be performed with commercially available current probes (e.g. LEM PR50 Universal 50 MHz current probe) without the use of any sophisticated circuits.

Conventional circuit 1

A first conventional voltage clamping circuit is shown in Fig 2.11. The circuit is connected to the drain and source terminals of the evaluated semiconductor device. The measurement of the drain-to-source voltage waveform is performed with an oscilloscope by placing a voltage probe between output nodes A and B. During the off-state, the drain voltage of the evaluated semiconductor device is high (e.g. 300 V) and the voltage between the output nodes A and B (V_{out}) is clamped to a level equal to the sum of the voltage drop across diode D_1 and the Zener voltage across diode D_2. The main reason for using diode D_1 is to reduce the value of the parasitic capacitance of diode D_2.

The value of the clamping voltage is chosen greater than the on-state voltage of the evaluated semiconductor device. Consequently, diodes D_1 and D_2 will not clamp the voltage during the on-state and the measured voltage V_{out} will be equal to the on-state voltage. Note that the highest measured voltage V_{out} is the clamping voltage. Consequently, the measurement range of the oscilloscope may be set to one wide enough to measure the clamping voltage instead of the high off-state voltage (e.g. 300 V). This results in an increase of the measurement resolution of the oscilloscope with a factor:

$$\text{Resolution improvement} = \frac{\text{Off} - \text{state voltage}}{\text{Clamping voltage}} \tag{2.14}$$

However, this circuit has some disadvantages. Fig. 2.12 shows that during the on-state there is a current flowing through the resistor R resulting in a voltage drop across it. Therefore, the measured voltage at the output of the circuit will be the on-state voltage minus a voltage drop across R. There is also an RC-time constant caused by the resistor R and the parasitic capacitances of diodes D_1 and D_2, and of the measurement probe. Due to this time constant, the output voltage of the circuit will only gradually decrease to the on-state voltage, causing a measurement delay. To counter this problem, the resistance value of R could be reduced. However, to limit the power dissipation of R, which shows a maximum during the off-state of the device, its value should not be chosen too low. Furthermore, the value of R also depends on the current which has to flow through D_2 in order to achieve correct Zener operation. Due

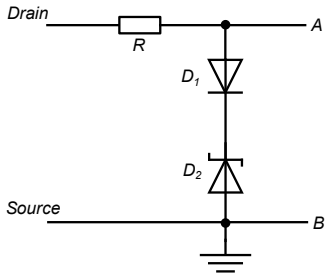


Figure 2.11: Conventional circuit 1.

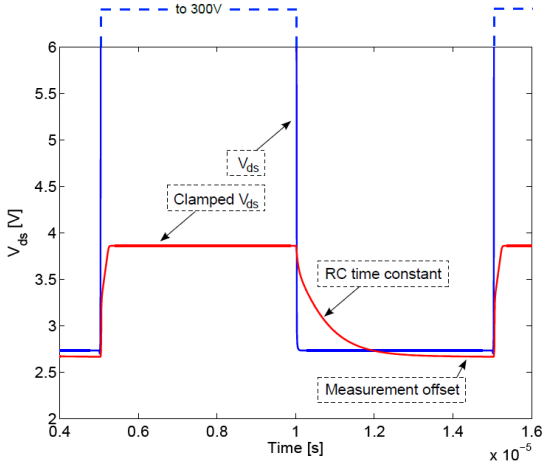


Figure 2.12: Simulation results of conventional circuit 1 (100 kHz).

to these disadvantages this circuit cannot be used to evaluate the on-resistance during high-speed operation. Only switching frequencies of a few tens of kHz are feasible.

Conventional circuit 2

A second conventional voltage clamping circuit is described in the US patent application 2008/0309355 A1 and is depicted in Fig. 2.13. The circuit is connected to the drain and source terminals of the semiconductor device. The on-state voltage is measured between the nodes A and B (V_{out}) using a voltage probe. Transistor T is a normally-on type field-effect transistor with a negative threshold voltage (e.g. -2 V). The gate of transistor T is connected to a DC voltage supply V_{cc}.

When a current flows through the resistor R the voltage drop across it causes an increase of the voltage at the source side of transistor T. At this point, when the voltage difference between the gate (e.g. 2 V) and the source of transistor T becomes lower than its threshold voltage (e.g. -2 V), transistor T is turned off, causing the output voltage V_{out} to be clamped to the clamping voltage $V_{clamp} = V_{cc} - V_{gs,th} = 4$ V. Therefore, the range of the oscilloscope may be set to one wide enough to measure V_{clamp}. When the evaluated semiconductor device is turned on, its drain voltage becomes lower than V_{clamp} and is measured at the output of the voltage clamp circuit. For a clamping voltage of e.g. 4 V, the measurement accuracy is $4/2^8 = 0.0156$ V, using an 8-bit resolution oscilloscope. This allows a sufficiently accurate measurement of an on-state voltage of e.g. 1 V.

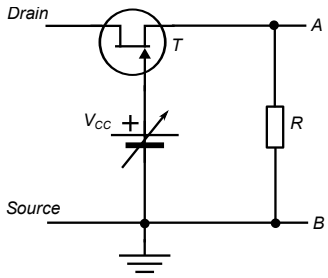


Figure 2.13: Conventional circuit 2.

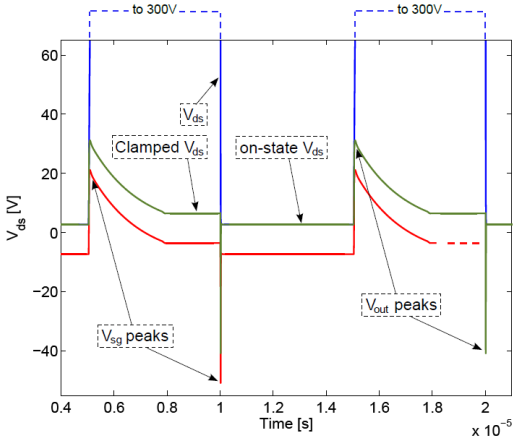


Figure 2.14: Simulation results of conventional circuit 2 (100 kHz).

This circuit also has some disadvantages. Firstly, Fig. 2.14 shows that if the drain voltage of the evaluated semiconductor device rises, the output voltage V_{out} is increased above V_{clamp} (V_{out} peaks) due to the parasitic drain-to-source capacitance of the normally-on type field-effect transistor T in combination with the relatively high value of a resistance R. This peak voltage can be several times the clamping voltage V_{clamp}, distorting the characteristics of an amplifier inside the oscilloscope, and resulting in failure to accurately measure the voltage waveforms. Moreover, the rise of the output voltage V_{out} will cause the gate-to-source voltage V_{gs} of the normally-on type field-effect transistor T to become more negative than allowed (V_{sg} peaks). This might destroy the normally-on type field-effect transistor T. However, this can be solved by putting a fast switching diode between the source and gate of the normally-on type field-effect transistor T.

Secondly, during the on-state of the semiconductor switching device, a small current flows through the normally-on type field-effect transistor T, causing a voltage drop across this transistor. This will introduce an error on the measurement.

Thirdly, during the transition to the off-state of the evaluated semiconductor device there is large dv/dt across the capacitance C_{gd} of T. Consequently, a large current will flow through the voltage supply V_{cc} what might lead to its destruction.

According to the US patent application 2008/0309355 A1, a wide gap normally-on type field-effect transistor should be used in the voltage clamp circuit (Fig. 2.13). However, this is not strictly required for the circuit to work.

By increasing the voltage V_{cc} by a few volts (e.g. $V_{cc} = 8$ V), also a regular normally-off type field-effect transistor can be used. This will yield a clamping voltage of $V_{clamp} = 6$ V when the threshold voltage is 2 V.

Novel voltage clamping circuit

Fig. 2.15 shows the presented voltage clamping circuit that consists of a current mirror (e.g. a Wilson or a cascode current mirror), two high voltage diodes having the same $I - V$ characteristics D_A and D_B (e.g. BAV 3004W) and a number of clamping diodes. The circuit is connected to the drain and source terminals of the evaluated semiconductor device. The output voltage waveform V_{out} of the circuit is measured between the nodes A and B using a differential probe and an oscilloscope. The Wilson current mirror provides two equal currents (mirror currents). The value of these currents is determined by R_E and R and the value of the DC voltage source as shown in Fig. 2.15.

During the on-state of the evaluated semiconductor device, these two mirror currents flow through the high voltage diodes D_A and D_B causing identical voltage drops across them. Therefore, the output voltage V_{out} measured between the nodes A and B is equal to the on-state voltage of the evaluated semiconductor device. During the off-state of the evaluated semiconductor device, diode D_A is reverse biased, forcing the current to flow through the clamping diodes. As a result, the output voltage V_{out} is clamped to the clamping voltage V_{clamp}, determined by the voltage drops across the clamping diodes.

Note that reversely connected Zener diodes can also be used as clamping diodes.

The value of the clamping voltage V_{clamp} can be adjusted by using a different number of clamping diodes. Because the output voltage V_{out} is limited to at most the clamping voltage V_{clamp}, the range of the oscilloscope may be set to one wide enough to measure V_{clamp}.

The presented voltage clamping circuit has a high measurement accuracy. Current mirrors typically exhibit a high current accuracy of ± 0.5 % (see for example the REF200 current mirror from Texas Instruments). When the mirror currents have for example a nominal value of 60 mA, in the worst case situation, the real mirror currents are 60.3 mA and 59.7 mA. In case two high voltage diodes BAV 21 are used, a PSpice simulation reveals that this will result in a difference between the voltage drops across the high voltage diodes D_A and D_B of about 0.983 mV. When the on-state voltage of the evaluated semiconductor device is for example 1 V, this means that the measurement error is at most 0.1 %.

Fig. 2.16 shows simulation results of the presented circuit. There are no voltage peaks at the output during the transition to the on-state. However, during the transition to the off-state there is a voltage of about 6.3 V which is still much less than the voltage peaks observed in the second conventional circuit. This

voltage peak is caused by the parasitic capacitance of diode D_A (BAV 3004W) and can be minimized by choosing a better diode. For the best performance a diode should be chosen with the lowest parasitic capacitance and with limited reverse recovery.

The Wilson current mirror topology is chosen to avoid the Early effect of the two upper BJT transistors. The top resistors in the Wilson current mirror are used to optimize the circuit so that it can deal with temperature differences, variations in transistor characteristics, etc. Also a cascode current mirror can be used to provide two equal currents.

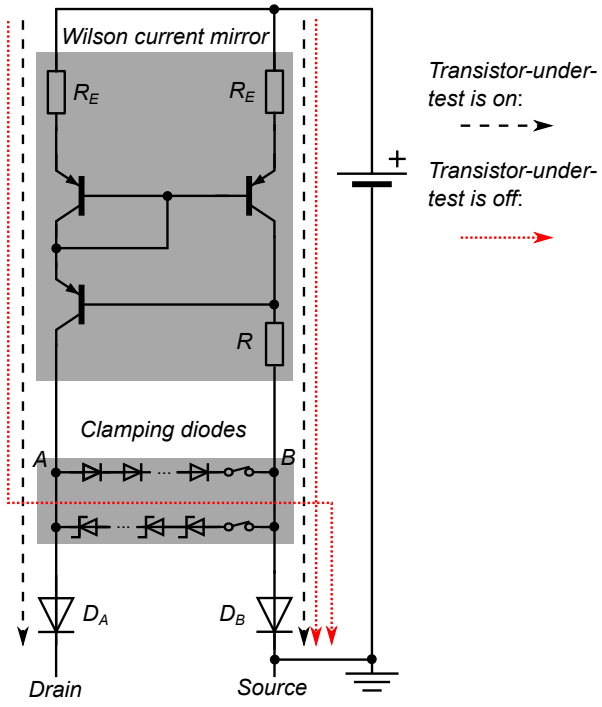


Figure 2.15: Novel voltage clamping circuit.

The main advantage of the presented voltage clamping circuit is that it does not introduce delay caused by RC-time constants keeping the voltage waveform clear even during state transitions of the evaluated semiconductor device.

Also, the measurement resolution improves drastically. For instance, if the off-state drain-to-source voltage is clamped from 300 V to 3.3 V , the measurement resolution is increased by a factor of $300/3.3 = 91$ times (eq. (2.14)). This is, however, a theoretical improvement as in practice the clamped voltage contains a voltage peak at the transition to the off-state of the semiconductor switching device. The value of this voltage peak depends on the switching times of the

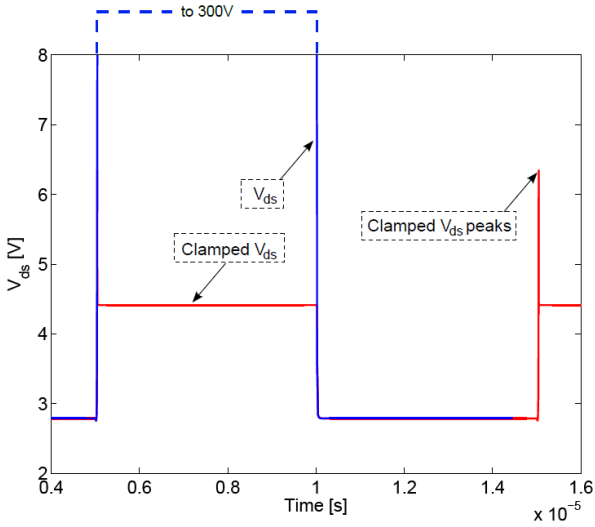


Figure 2.16: Simulation results of the novel voltage clamp circuit (100 kHz).

semiconductor switching device and the parasitic capacitance of the high voltage diode connected to the drain of the semiconductor switching device.

After the instantaneous dynamic on-resistance has been determined with equation (2.13), a single, representative, value for it can be calculated for instance on an energy basis, using following equation:

$$R_{on,dyn,avg} = \frac{1}{I^2 T_{on}} \int_0^{T_{on}} R_{on,dyn}(t) \cdot i^2(t) dt \quad \text{with} \quad I = \frac{1}{T} \int_0^{T} i(t) dt \quad (2.15)$$

where i is the instantaneous current through the transistor, $R_{dyn,on}(t)$ is the instantaneous dynamic resistance, T_{on} is the time duration where the transistor is in its on-state and T is the switching period.

The presented voltage clamping circuit has been patented [Drie 11].

Conclusion about measuring the dynamic on-resistance

Conventional circuits for measuring the on-state voltage waveform of a transistor exhibit a number of problems such as an RC-time constant, measurement offset, undesired voltage peaks due to parasitic coupling elements etc. As a result, the measured on-state voltage waveform contains a measurement error and/or has a low measurement resolution. To address these problems a novel voltage clamping circuit, improving the accuracy of the on-state voltage waveform measurement, is proposed in this work. The presented voltage clamping circuit does not introduce any delay caused by an RC-time constant keeping the voltage

waveform clear even during state transitions of the semiconductor switching device for frequencies up to 1 MHz and higher. The novel voltage clamping circuit drastically improves the measurement resolution of the on-state voltage waveform.

Quantifying the accuracy of the measurement circuit

In a previous paragraph, a numerical example illustrated the accuracy of the voltage clamping circuit. Making use of the relationships between voltage and current of diodes, an expression for the absolute and relative errors can be derived. Referring to Fig. 2.15, it is assumed that diode D_A is a p-n-diode, conducting a current I, and having a junction at temperature T. Diode D_B is a p-n-diode, conducting a current $I + \Delta I$ and having a junction at temperature $T + \Delta T$. Suppose the saturation currents of both diodes are the same, and are I_0. The absolute error ϵ of the on-state voltage is then the difference of the two p-to-n voltages of the diodes:

$$\epsilon = V_{pn,A} - V_{pn,B}$$

For p-n-diodes, the relationship between p-to-n-voltage and diode current is [Zegh 09]:

$$I = I_0 \left(e^{V_{pn,A}/(nV_{t,A})} - 1 \right) \tag{2.16}$$

$$I + \Delta I = I_0 \left(e^{V_{pn,B}/(nV_{t,B})} - 1 \right) \tag{2.17}$$

with $V_{t,A} = kT/q$ and $V_{t,B} = k(T + \Delta T)/q$. Therefore, the error is:

$$\begin{aligned} \epsilon &= V_{pn,A} - V_{pn,B} \\ &= \frac{nkT}{q} \ln\left(\frac{I}{I_0} + 1\right) - \frac{nkT}{q} \ln\left(\frac{I + \Delta I}{I_0} + 1\right) - \frac{nk\Delta T}{q} \ln\left(\frac{I + \Delta I}{I_0} + 1\right) \\ &= \frac{nkT}{q} \ln\left(\frac{\frac{I+I_0}{I_0}}{\frac{I+\Delta I+I_0}{I_0}}\right) - \frac{nk\Delta T}{q} \ln\left(\frac{I + \Delta I}{I_0} + 1\right) \end{aligned}$$

Neglecting I_0 with respect to I, we find:

$$\epsilon \approx -\frac{nkT}{q} \ln\left(1 + \frac{\Delta I}{I}\right) - \frac{nk\Delta T}{q} \ln\left(\frac{I + \Delta I}{I_0} + 1\right)$$

Making use of the Maclaurin-series of the natural logarithm $\ln(1+x) \approx x, x \to 0$, we have:

$$\epsilon \approx -\frac{nkT}{q}\frac{\Delta I}{I} - \frac{nk\Delta T}{q}\frac{V_{pn,B}}{nkT/q} = -\frac{nkT}{q}\frac{\Delta I}{I} - \frac{\Delta T}{T}V_{pn,B} \tag{2.18}$$

At 300 K, with $\Delta I = 0.6$ mA, $I = 59.7$ mA, and for two BAV 21 diodes that are held at the same temperature, and have an emission coefficient of $n = 2.233$[1], we find an absolute error of

$$\epsilon \approx -\frac{2.233 \cdot 1.38065 \cdot 10^{-23} \cdot 300}{1.602 \cdot 10^{-19}} \frac{0.6}{59.7} = -0.5824 \text{ mV}$$

approximating the value simulated by PSpice, stated above.

Dynamic on-resistance

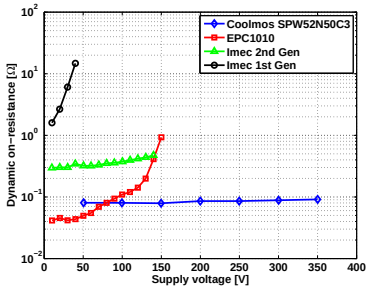
The dynamic on-resistance, that is, the resistance while the device is operating inside the power converter, is measured. The voltage clamping circuit with current mirror is employed. A Tektronix P6250 differential voltage probe (500 MHz) is used for measuring the output voltage and a LEM PR50 current clamp probe (50 MHz) is used for measuring the current through the coil, which also passes through the transistor during its on-state. The instantaneous value of the dynamic on-resistance is averaged with formula (2.15). Four types of experiments are conducted. In experiment A (Fig. 2.17a), the resistance is measured in function of the supply voltage. In experiment B (Fig. 2.17b), the current through the transistor varies. In experiment C (Fig. 2.17c), the duty cycle varies and in experiment D (Fig. 2.17d), the switching frequency varies. The parameters that are kept constant in each experiment are listed in Table 2.5, for each of the devices that are measured. In the Table, I_{ds} is the current which flows through the transistor while it is in its on-state and V_{ds} is the voltage across drain and source while the transistor is in its off-state. In part (b), (c) and (d) of the Figure, the y-axes on the right should be used for Imec's second generation device.

Imec's first generation device was destroyed at 48 V during experiment A, due to the very high on-resistance due to charge trapping effects and subsequent heating of the device. The Coolmos is not influenced by charge trapping effects; this is mainly a problem in AlGaN/GaN HEMTs. Up to now, no theoretical model has been derived for expressing the relationship between the dynamic on-resistance and V_{ds}. The charge trapping effect is also not included in the Spice device models, so a comparison with simulation results is not sensible. However, it is important to measure the dynamic on-resistance in order to know the high-frequency figure of merit (BHFFOM) for all these transistors. As can be seen from Figs. 2.17c and 2.17d, the on-resistance of the GaN-devices decreases with duty cycle and increases with switching frequency. This is expected, because of the mechanism of charge trapping. However, Fig. 2.17b also shows a not so trivial behaviour: when I_{ds} increases, the dynamic on-resistance first decreases and then increases.

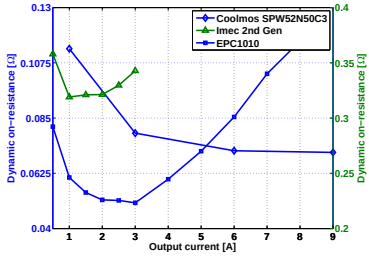
[1]The emission coefficient is obtained from the Spice-model of the diode.

Table 2.5: Experiments for measuring the dynamic on-resistance of various devices.

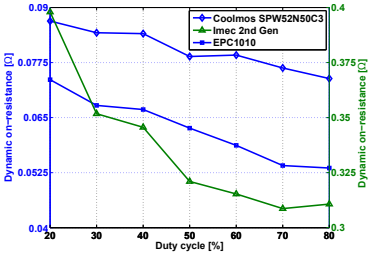
Parameters that are kept constant	**Coolmos SPW52N50C3**	**Imec First Gen. GaN**	**Imec Second Gen. GaN**	**EPC1010**
Experiment A	V_{gs} = 0/15.662 V, f_s = 150 kHz, δ = 50 %, I_{ds} =3 A	V_{gs} = 0.563/-7.882 V, f_s = 300 kHz, δ = 50 %, I_{ds} = 1.5 A	V_{gs} = 0.563/-7.882 V, f_s = 300 kHz, δ = 50 %, I_{ds} = 1.5 A	V_{gs} = 4.475/-2.51 V, f_s = 300 kHz, δ = 50 %, I_{ds} = 1.5 A
Experiment B	V_{gs} = 0/15.662 V, f_s = 150 kHz, δ = 50 %, V_{ds} = 149.86 V		V_{gs} = 0.563/-7.882 V, f_s = 300 kHz, δ = 50 %, V_{ds} = 50 V	V_{gs} = 4.48/-2.55 V, f_s = 300 kHz, δ = 50 %, V_{ds} = 50 V
Experiment C	V_{gs} = 0/15.662 V, f_s = 150 kHz, V_{ds} = 150 V, I_{ds} = 3 A		V_{gs} = 0.563/-7.882 V, f_s = 300 kHz, V_{ds} = 50 V, I_{ds} = 1.5 A	V_{gs} = 4.475/-2.51 V, f_s = 300 kHz, V_{ds} = 50 V, I_{ds} = 1.5 A
Experiment D	V_{gs} = 0/15.662 V, δ = 50 %, V_{ds} = 150 V, I_{ds} =3 A		V_{gs} = 0.563/-7.882 V, δ = 50 %, V_{ds} = 50 V, I_{ds} = 1.5 A	V_{gs} = 4.475/-2.51 V, δ = 50 %, V_{ds} = 50 V, I_{ds} = 1.5 A



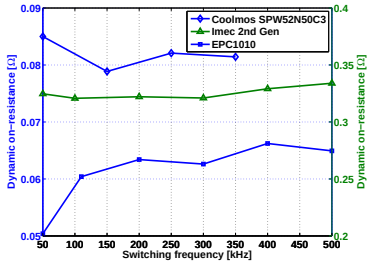
(a) Dynamic on-resistance versus supply voltage.



(b) Dynamic on-resistance versus output current.



(c) Dynamic on-resistance versus duty cycle.

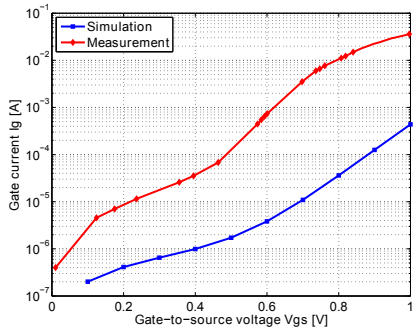


(d) Dynamic on-resistance versus switching frequency.

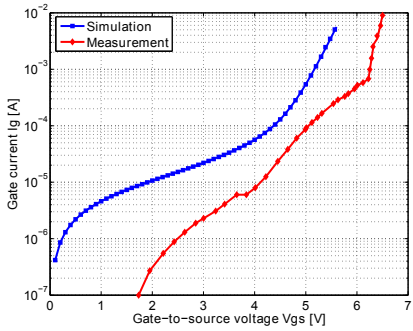
Figure 2.17: Dynamic on-resistance measurements.

2.3.3 Gate current in function of gate-to-source voltage

Many HFETs have JFET-like structures and in such structures, there is a parasitic diode between gate and source. This means that a current will flow when a voltage is applied between gate and source. Another implication is that the gate-voltage has a maximum value, corresponding to the maximum allowed gate leakage current. Power electronic designers thus have to take this maximum voltage and the loss due to the leakage current into account and the measurement of this characteristic is thus of importance to them. For Imec's second generation device and for the EPC component, these characteristics are measured and compared with PSpice simulations (Fig. 2.18a-2.18b). It can be seen that the Spice-model does not accurately predict the gate current at all. The current and the voltage are measured with two Keithly 2000 multimeters. The measurement and simulation are performed at 23 degrees Celsius for both the EPC component and for Imec's second generation device. For the EPC component, there is a protective Zener diode (V_Z=5.6 V) between gate and source and also a resistor of 100 kΩ, but even with these components present the leakage currents is lower than simulated. No measurements were done for the Coolmos because its gate is isolated from the source; no diode is present here between gate and source.



(a) Gate leakage current versus gate-to-source voltage for Imec's second generation device.



(b) Gate leakage current versus gate-to-source voltage for EPC's device.

Figure 2.18: Gate leakage current versus gate-to-source voltage.

2.3.4 Gate charge

The total and Miller gate charge of the Coolmos device, EPC1010 and Imec's second generation GaN-transistor, and the comparison with the results from a Spice simulation, are shown in Fig. 2.19a-2.19f. A high-ohmic gate resistor

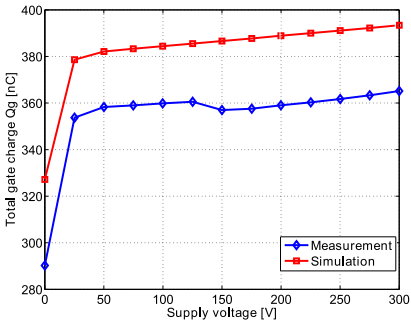
is used in the gate-driver (22 Ω for the Coolmos, 268.54 Ω for EPC1010 and 269.5 Ω for Imec's second generation device) because it is desirable to turn the transistors slowly on and off, in order to be able to perform the measurements with greater accuracy. However, a slower switching leads to greater switching losses. Hence, the switching frequency during these experiments should be low (Coolmos: 150 kHz, Imec's second generation device: 100 kHz, EPC1010: 110 kHz). In all cases, the duty cycle is 50 %. V_{gs} is a rectangular wave between 0 and 15.662 V for the Coolmos, between -7.4 and 0.85 V for Imec's second generation device and is between -2.51 and 4.475 V for the EPC1010-device. I_{ds} is 3 A for the Coolmos, 1.5 A for Imec's second generation device and 1.5 A for the EPC1010-device.

The current through the gate resistors is measured with the Tektronix differential voltage probe P6250 and integrated over the time, yielding the charge. This charge needs to be measured because it is one of the two factors in the high-frequency figure of merit (BHFFOM). The Miller charge is proportional to V_{ds} as can be seen from the measurement results. This is also theoretically true.

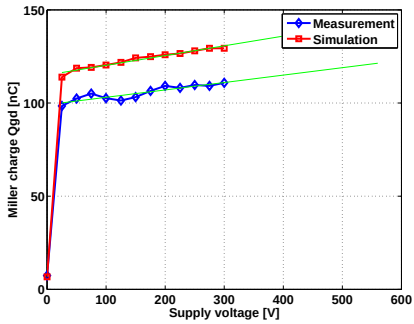
The higher the supply voltage V_{DD} is, the more voltage is across C_{gd} and the more charge should be extracted from this capacitor to discharge it. In Fig. 2.19b, 2.19d and 2.19f, it can be seen that the Miller charge Q_{gd} is proportional to the supply voltage V_{DD} in a specific voltage range. When the gate-driver supplies a constant current, this linear behaviour implies that the small-signal Miller capacitance C_{gd} is almost constant in that voltage range. Inspection of the datasheet of the Coolmos component reveals that $C_{gd} = C_{rss}$ is equal to 55 pF for voltages higher than 100 V, and remains approximately constant. Therefore, when the voltages increases from 100 to 300 V, the Miller charge increases with 200 V·55 pF = 11 nC. This is indeed the case as can be seen in Fig. 2.19b. In general, the Miller charge Q_{gd} is not exactly proportional with V_{DD}. Actually, the dependency is $Q_{gd} = C_{gd,0}\left(1 - k\sqrt{V_{DD} - V_{miller}}\right)(V_{DD} - V_{miller})$ with k a constant, V_{miller} the voltage at the Miller platform and $C_{gd,0}$ the gate-to-drain capacitance at a drain-to-source voltage of zero Volt. The reason for this is that the gate-to-drain capacitance is proportional to $1 - k\sqrt{V_{ds}}$, with k a constant [Oh 00].

Except for Imec's second generation device and the Coolmos, the measurements agree well with the simulation results. It can be concluded that for Imec's device and for the Coolmos, the Spice models do not very accurately model the gate charge and hence, in general, one should be careful when using Spice models for determining the gate charge.

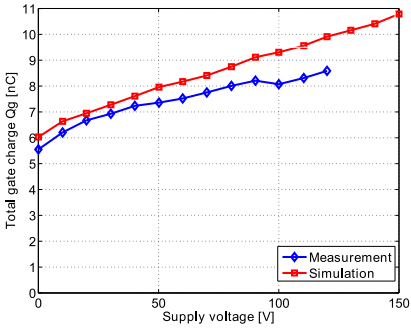
Figs. 2.20a-2.20c show the Miller (platform) voltage. The threshold voltage of an n-channel transistor is slightly less. Therefore, it can be seen from Fig. (c) that Imec's second generation device is normally-on.



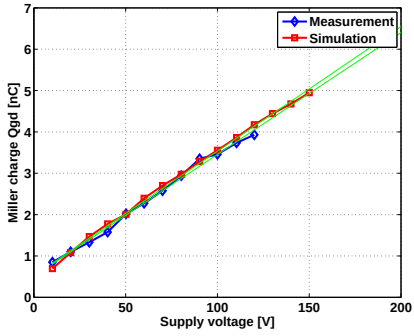
(a) Total gate charge versus supply voltage for the Coolmos.



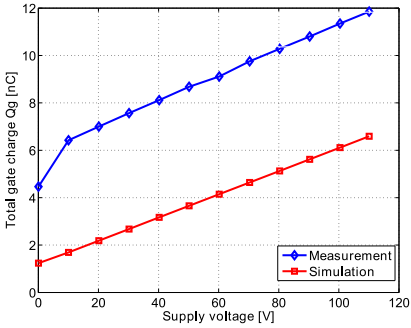
(b) Miller charge versus supply voltage for the Coolmos.



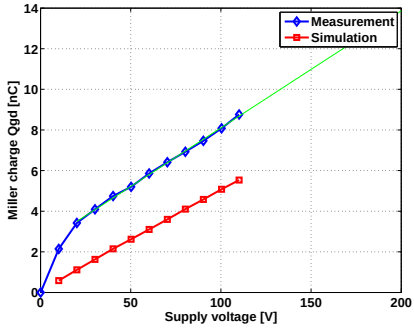
(c) Total gate charge versus supply voltage for the EPC-device.



(d) Miller charge versus supply voltage for the EPC-device.

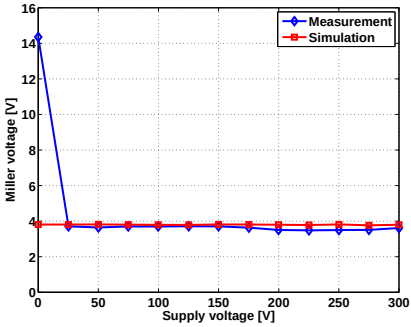


(e) Total gate charge versus supply voltage for Imec's second generation device.

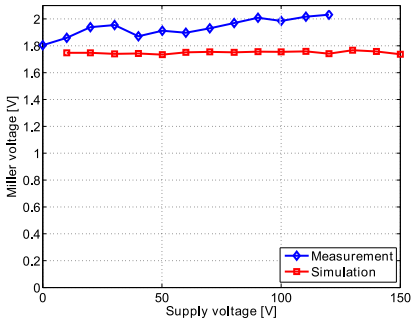


(f) Miller charge versus supply voltage for Imec's second generation device.

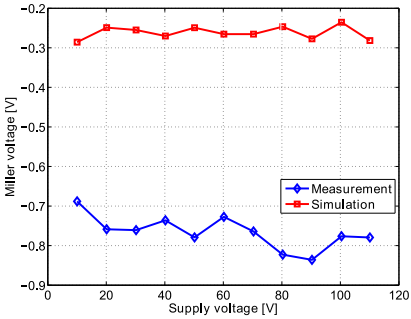
Figure 2.19: Gate charge measurements.



(a) Miller voltage versus supply voltage for the Coolmos.



(b) Miller voltage versus supply voltage for the EPC-device.



(c) Miller voltage versus supply voltage for Imec's second generation device.

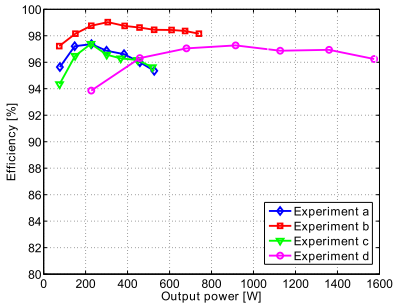
Figure 2.20: Miller voltage versus supply voltage.

2.3.5 Efficiency

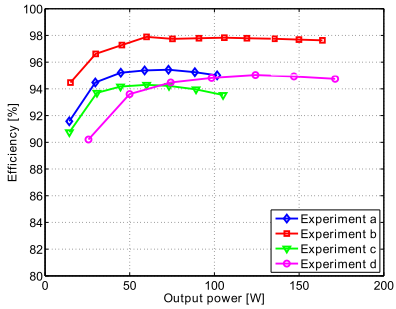
In order to investigate how the semiconductor switching device influences the efficiency of the entire converter, four types of efficiency measurements are conducted. Experiment B differs from experiment A in the fact that the duty ratio is increased. However, both of these experiments are conducted at the same switching frequency and current through the transistor. Experiment C differs from experiments A and B in the fact that the switching frequency in C is much higher. In experiment D, the switching frequency and duty ratio are the same as in experiment A, but now, the current is higher. The exact parameters for these experiments are listed for the Coolmos, Imec's second generation GaN device and for the EPC1010-transistor in Table 2.6. I_{ds} is the drain current through the transistor when it is on, δ is the transistor's duty ratio, f_s its switching frequency and T_a is the ambient temperature. All the experiments are conducted with a gate-resistor of 2.2 Ω and every time, the

output voltage of the converter is varied.

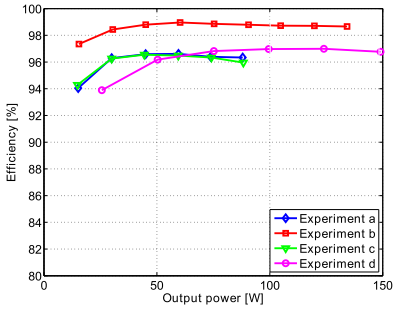
The efficiency is measured with a Voltech PM3000A Three-Phase Power Analyzer and the results are depicted in Fig. 2.21a, 2.21b and 2.21c. It can be seen that the choice of the transistor influences the overall efficiency a lot. The converter is 1 to 2 % more efficient when EPC's HEMT is used instead of Imec's HEMT. Fig. 2.21d finally shows the efficiency versus the switching frequency, in the converter where the EPC1010 is used, with $\delta = 50$ %, $I_{ds} = 1.5$ A and for a constant output voltage of 30 V.



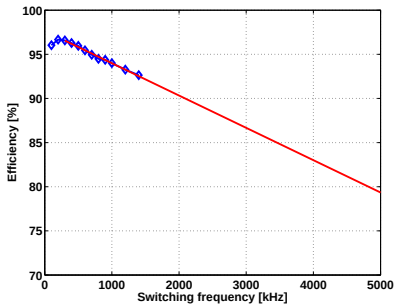
(a) Efficiency versus output power for the Coolmos.



(b) Efficiency versus output power for Imec's second generation device.



(c) Efficiency versus output power for the EPC-device.



(d) Efficiency versus switching frequency for the EPC-device.

Figure 2.21: Efficiency measurements.

Table 2.6: Parameters in the four experiments for measuring the efficiency.

	Coolmos SPW52N50C3				**Imec's 2nd Gen. GaN**				**EPC1010**			
	A	**B**	**C**	**D**	**A**	**B**	**C**	**D**	**A**	**B**	**C**	**D**
$\mathbf{f_s}$ [kHz]	150	150	300	150	150	150	300	150	150	150	300	150
$\boldsymbol{\delta}$ [%]	50	80	50	50	50	80	50	50	50	80	50	50
$\mathbf{I_{ds}}$ [A]	3	3	3	9	1.5	1.5	1.5	2.5	1.5	1.5	1.5	2.5
$\mathbf{T_a}$ [°C]	NA	NA	NA	NA	25	26	26	26	25.9	26	26	26

2.3.6 Maximum frequency

For determining the maximum frequency of a transistor, used in the switching operation mode, no generally accepted definitions or methods exist. In contrast, when the transistor is used as an amplifier, a *transition frequency* f_T can be defined as a measure for its maximum operating frequency. For bipolar junction transistors, it is the frequency where the small-signal current gain i_c/i_b becomes equal to 1. i_b is the small-signal base current and i_c the small-signal collector current. For MOSFETs, the transition frequency is the frequency where the small signal current gain i_d/i_g becomes 1, when the drain and source terminals are both connected to the small-signal ground. Here, i_d is the small-signal drain current and i_g is the small-signal gate current. However, when the transistor is used as switch, as is the case in power electronics, and not as amplifier, no generally accepted definitions for a maximum frequency exist. Three ways to define a maximum operating frequency for a switching transistor are:

- When the efficiency of the converter becomes too low, the switch reaches its maximum frequency.
- When the rise and fall time of the drain-to-source voltage waveform take a too large portion of the switching period T, it can be concluded that the switch reaches its maximum frequency.
- When the transfer function of the power converter deviates too much from its theoretical value at low frequency, the switch reaches its maximum frequency. For instance, in the case of the reversed buck converter operating in continuous conduction mode, the transfer function, i.e. the ratio of the output and input voltages, is $V_{out}/V_{in} = \delta$, with δ the duty ratio. In case of a 50 % duty ratio, the output voltage is half of the input voltage. At higher switching frequencies, the drain-to-source voltage is not so much rectangular anymore, but more trapezoidal and has increased rise and fall times. Also, because of increased switching losses, the junction temperature and the on-resistance increase and a larger voltage drop is present across the switch in its on-state. More losses also mean that less energy is being transferred to the output. Furthermore, capacitive effects in the coil and inductive effects in the capacitors become more important. All these effects cause the output voltage to be different from its theoretical value. When the deviation is too large, the transistor reaches its maximum frequency.

But what is a 'too low' efficiency, a 'too large' deviation from the theoretical transfer function, what is a 'too high' fraction $(t_{rise}+t_{fall})/T$? That is something that has to be quantified in a rather arbitrary manner.

For Imec's second generation GaN device, these three quantities have been measured in the reversed buck converter for a constant input voltage of 65 V, a duty ratio of 50 %, an average input current of 0.75 A and at an ambient temperature of 27.2 °C (Fig. 2.22). For instance, if one defines the maximum frequency of a switch as the point where $t_{rise} + t_{fall}$ takes up 20 % of the period T, Imec's GaN device has a maximum frequency, for this particular combination of converter layout and gate-driver, of a little bit more than 4 MHz.

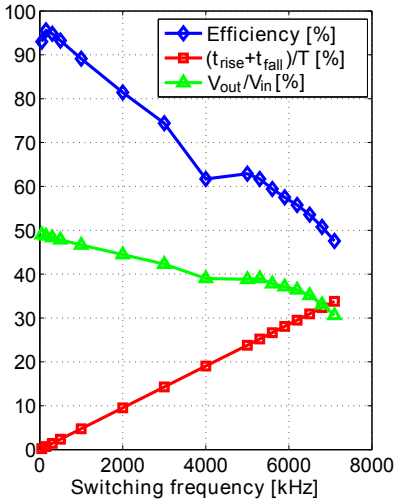


Figure 2.22: Determining the maximum frequency of Imec's second generation device.

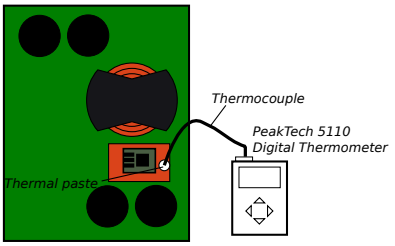
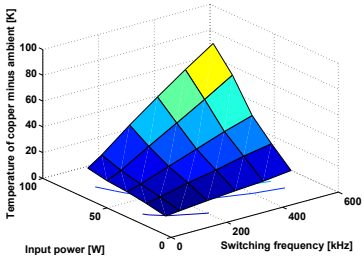


Figure 2.23: Measuring the temperature of the copper carrier plate of Imec's GaN transistor.

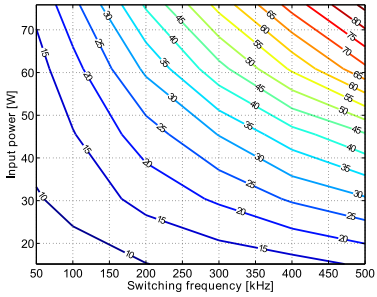
2.3.7 Thermal measurements

Switching losses increase linearly with the switching frequency [Moha 02], and consequently, the temperature increases of the copper plate that is present between the AlN-carrier of Imec's second generation GaN transistor and the copper heat spreader attached to the heat sink. This temperature is measured with a K-series thermocouple connected to a PeakTech 5110 Digital-Thermometer. At each measurement point, a sufficiently long time is waited until thermal equilibrium is reached, before the measurement is recorded. The temperature of the copper plate minus the ambient temperature is shown in Figs. 2.24a-2.24d, in function of the switching frequency and the input power of the converter. Also, the temperature of the AlN-carrier is measured. This is not done with a thermocouple, but with a FLIR A40 thermal imaging camera. The thermal image is shown in Fig. 2.25 for an input voltage of 100 V, for $I_{ds} = 1.5$ A, for a duty ratio of 50 % and for a switching frequency of 500 kHz.

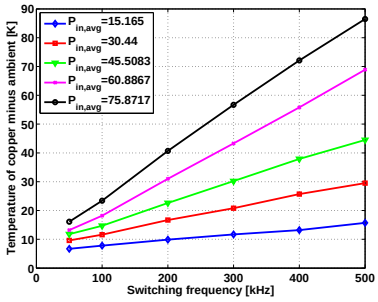
The camera is calibrated and records a temperature of 113.0°C at point $SP01$, 114.0°C at point $SP02$, 111.9°C at point $SP03$ and 113.9°C at point $SP04$. These thermal techniques can be useful for determining up to which maximum frequency, from a thermal point of view, the converter can be used.



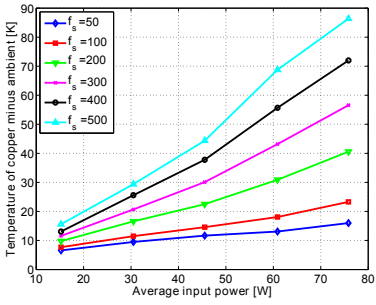
(a) Heating in function of switching frequency and average input power: 3D-plot.



(b) Heating in function of switching frequency and average input power: contour plot.



(c) Heating versus switching frequency, for different input powers (W).



(d) Heating versus average input power, for different switching frequencies (kHz).

Figure 2.24: Heating of copper heat spreader above ambient temperature.

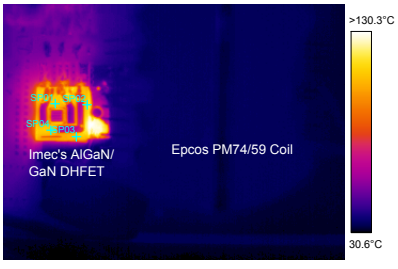


Figure 2.25: Thermal measurements with a FLIR camera of Imec's second generation device.

2.3.8 Figure of merit

The inverse of the dynamic figure of merit, $Q_{gd}R_{on,dyn}$, (a modification of eq. (2.4)) is shown for the Coolmos, EPC1010 and Imec's second generation GaN-device in Fig. 2.26, in function of the supply voltage of the reversed buck converter. A lower product $Q_{gd}R_{on,dyn}$ means that the device has less conduction and switching losses. The breakdown voltage of Imec's second generation device was determined to be about 200 V. In order to compare Imec's 200 V device, and the EPC1010 (also a 200 V device) with other 200 V-devices (MOSFETs), $Q_{gd}R_{on,stat}$ is listed in Fig. 2.27. Only two 550 V-devices are present in that Figure. This Figure is drawn based on the data of Table A.1 of Appendix A. It can be seen that the EPC1010-device has the best efficiency and that Imec's device does not perform too well for a wide-bandgap semiconductor device. Except for the GaN devices, the static on-resistance is taken from the datasheets of the devices for $V_{gs} = 10$ V. The Miller charge of the MOSFETs is taken from the datasheet at $V_{ds} = 100$ V. When it is given in the data sheet at another voltage, a linear interpolation is used in order to refer it to 100 V. This is possible because in this Chapter it is shown that Q_{gd} and V_{ds} are proportional to each other.

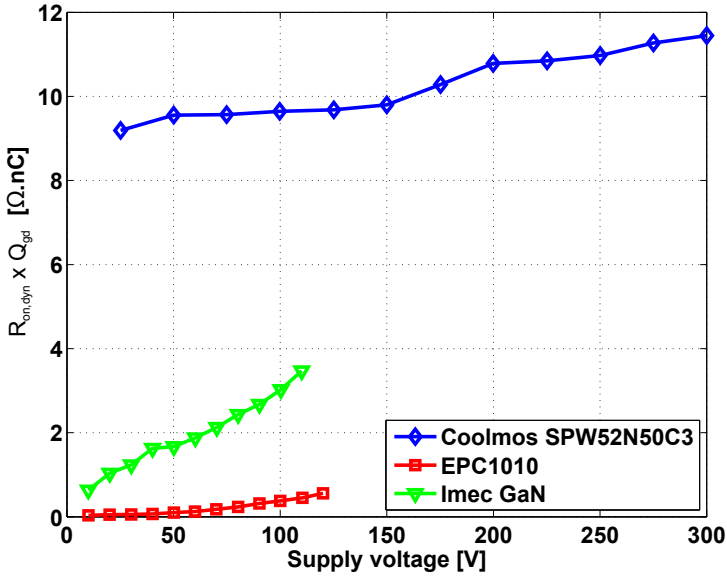


Figure 2.26: $Q_{gd}R_{on,dyn}$, inverse of the dynamic figure of merit, versus supply voltage.

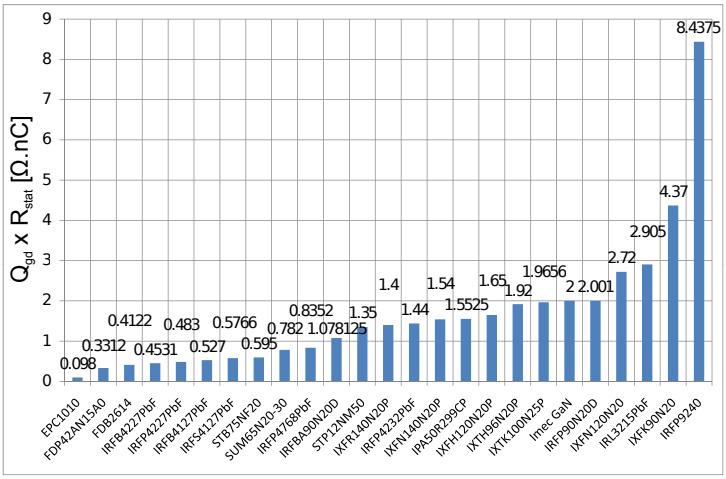


Figure 2.27: Inverse of the static figure of merit, $Q_{gd}R_{on,stat}$, for different devices.

2.4 Conclusion

This doctoral work researches possible ways to increase the switching frequency in power converters and techniques to model the effects this increased switching frequency has on the components of the converter and of nearby electronic circuits. An increased switching frequency has many advantages such as a decreased size, a faster dynamic transient performance, and the possibility to manufacture inductive components or even entire circuits in a batch process by employing integrated components. A first manner to increase the switching frequency is by using transistors, built out of novel semiconductor materials, known as wide-bandgap (WBG) semiconductors. In this Chapter, first of all, important electrical and thermal material properties of some wide-bandgap semiconductors are given. Also, it is discussed why a higher bandgap than silicon gives these materials some advantages for use in power devices. One advantage is that their size can be decreased with respect to that of silicon devices and that the thinner devices can still withstand the same voltage. Smaller devices have lower capacitances because of their reduced size and can thus be switched on and off at faster speeds; that is why this Chapter discusses these semiconductor devices. Another benefit of a larger bandgap is that for a specific temperature, the intrinsic carrier density is lower and therefore the leakage current is lower, thus enabling wide-bandgap devices to be employed at higher junction temperatures.

Gallium nitride (GaN) is a promising WBG-material, and the power devices

constructed from GaN are often fabricated as high electron mobility transistors (HEMTs). The relationship is shown between the breakdown voltage and the specific on-resistance of power devices fabricated from different semiconductors. The relationship is dependent on material characteristics such as the critical breakdown field strength and the permittivity, and therefore a figure of merit can be defined, comparing the specific on-resistance of different semiconductor materials with each other, for the same breakdown voltage. This is a way of quantifying the performance of semiconductors. It can be seen that the figure of merit of GaN is a factor 671 better than silicon and a factor 5.2 better than silicon carbide (4H-SiC).

Previous figure of merit quantifies the conduction losses of power devices, but for a high-frequency operation, it is even more important to examine and compare switching losses.

The total losses in a power device are the sum of conduction and switching losses and are dependent on the chip area of the power switch. The larger the area, the lower the conduction losses, but the more charge is required to turn the device on or off. So, there exists an optimal area which minimizes the total losses. It turns out that these minimum losses are dependent on the square root of the product of the specific on-resistance and the specific switching charge [Bali 89]. This product is the inverse of a second figure of merit, called the high-frequency figure of merit, and it is shown that its value for GaN is 81 times bigger than for silicon. One can thus roughly say that losses in a GaN switch are $\sqrt{81} = 9$ times smaller than in a silicon switch of a comparable size.

The micro-electronics company Imec developed GaN power technology. The performance of Imec's devices, which are double-heterostructure HEMTs, was characterized in this work and compared with competing technology. We chose to do the tests in a commonly used converter, a reversed buck converter. A fast gate-driver is designed to operate the transistors. This gate-driver has to be fast for this project, providing the gate with a rectangular signal of multiple megahertz. Also, the driver has to be robust, so that if normally-on devices are tested, they are switched off in case there is an error in the control signal of the gate-driver. A third requirement for the gate-drivers is that the levels of the voltage pulses can be adjusted.

With the setup of the reversed buck converter and the developed gate-driver, the performance of Imec's GaN devices is assessed. Their characteristics are compared with a commercial superjunction device and with the first commercially available GaN HEMT, developed by EPC Corporation. The purpose of these measurements is to determine the high-frequency figure of merit for Imec's devices and compare it with that of the other devices. However, also other electrical characteristics are measured in order to get a more detailed idea of the performance of the device. First of all the static on-resistance is measured in function of the drain current. Pulsed measurements are used, in

order not to heat up the device too much. Then, the on-resistance is measured in function of the gate-to-source voltage. Next, the dynamic on-resistance is measured for different supply voltages. The dynamic resistance can differ from the static resistance because of the current collapse mechanism in HEMTs. Also, it is desirable to know the dynamic on-resistance because it depends on the junction temperature which is simply unknown. There is a resolution problem when measuring the dynamic on-resistance in a straightforward manner. If the measurements are done with a probe and an oscilloscope, the entire waveform of the drain-to-source voltage must fit in the oscilloscope screen, even though only the on-voltage is important. If one 'clips' the off-voltage on the scope, the internal amplifiers in the scope become saturated and when they recover too slowly from the saturation state, the measurements are distorted. However, the A/D-converters of the scope typically only offer 8 bits of resolution, which is much too low to accurately measure on-voltages of the order of 0.1 V. For this reason, a novel measurement circuit, based on a current mirror circuit, is developed, built and used, and this is patented as well. It is seen that the dynamic on-resistance of Imec's devices is very much dependent on the supply voltage, and only because of the use of surface passivation and field plates, it is able to operate at voltages higher than 60 V.

Also the efficiency of the reversed buck converter is measured under different operating conditions of current, duty ratio and switching frequency. A maximum switching frequency is determined, based on three possible definitions: the frequency where the sum of rise and fall times of the drain-to-source voltage takes up a too large fraction of the period, the frequency where the efficiency of the converter drops below a certain value, or the frequency where the transfer function differs too much from the ideal value. It is seen that, when taking the first definition, Imec's GaN devices have a maximum frequency of about 4 MHz.

Finally, datasheets of commercial devices with a comparable voltage or current as Imec's and EPC's devices, are used to determine the high-frequency figure of merit. This figure of merit makes however use of the total on-resistance and Miller charge, not of the specific values where a normalization with the chip area is applied. It is seen that EPC's device ranks best, but that Imec's device still can be improved.

To conclude, this Chapter offers an introduction to wide-bandgap power devices, which are useful for high frequency operation because of their intrinsic semiconductor properties. Wide-bandgap devices offer the possibility to build fast hard-switching power converters. The Chapter introduces the HEMTs manufactured by Imec and EPC. These are then characterized from a power engineer's point of view. A novel clamping circuit for measuring the dynamic on-resistance is presented. The high-frequency figure of merit of Imec's and EPC's devices is determined and compared with that of commercial devices of similar power and voltage ratings.

3

Design and Construction of a High-Frequency Zero Voltage Switching Resonant Converter

3.1 Introduction

3.1.1 Aims and specifications

This doctoral work is about high-frequency power electronics. It investigates how to build power converters operating at high switching frequencies. Some advantages of high-frequency power converters are [Fins]:

- At higher switching frequencies, energy is processed more often, so it can be handled in smaller quantities. This means less temporary energy storage so the passive components, responsible for storage, can shrink in size. These components occupy the bulk of the space in a converter, implicating that the use of higher switching frequencies *increases the power density*, possibly by orders of magnitude with respect to the current commonly-used technologies.
- The *transient response speed* of a converter is the speed by which the converter can adapt to changes in load or supply, or even in the control signals. Increasing the switching frequency means a faster transient response, making the control problem a lot easier.
- Because heavy components can be eliminated at higher switching frequencies, such as transformers with a heavy and big magnetic core, converters employing higher switching frequencies contain smaller and lighter inductors and transformers, possibly without a core, using only air, or employ integrated inductors, resulting in an *increased reliability* and resistance against mechanical shocks and vibrations. Furthermore, the elimination of electrolytic capacitors allows the high-frequency converters to operate at elevated ambient temperatures.
- At very high switching frequencies, discrete inductors or through-hole components are no longer required, and power converters can be manufactured using only surface-mounted components, allowing a fast *batch manufacturing process*, resulting in high repeatability and low cost.

One of the important opportunities while using higher switching frequencies, is that the size of the passive components can decrease. The inductance and capacitance values are inversely proportional to the switching frequency. But how is the *volume* of these components and of converters in general related to the frequency? In [Perr 09], it is shown that the volume of converters first decreases with $f_s^{-3/2}$, with f_s the switching frequency, and then with $f_s^{-1/2}$. Then, when the frequency further increases, the core losses of inductors become problematic and a decreasing core volume cannot get cooled enough, so the volume needs to increase again. It is assumed in this article that the volume

of the converter is determined by the volume of its inductors. The volume is proportional to $f_s^{-3/2}$ for a constant efficiency (Q: quality-factor) and to $f_s^{-1/2}$ for a constant heat flux.

In the previous Chapter, it was explained that wide-bandgap semiconductor components can be of great value in obtaining the important goal of increasing the switching frequency. These components can be made smaller than traditional silicon components, for the same power and temperature ratings, and therefore require less gate-charge to turn them on or off. Therefore, faster switching frequencies can be obtained.

However, the possibility of increasing the switching frequency is completely attributed to the intrinsic properties of these new semiconductor materials. It would also be interesting to investigate how to increase the frequency with the current silicon devices. In this case, new switching strategies should be explored, as opposed to the classical 'hard-switching' techniques. Both resonant and quasi-resonant techniques are of importance, as will be discussed in subsequent Sections. In this Chapter, a resonant converter will be designed and built. The importance of this work lies in the optimization of the design: the values of the elements of the resonant tank are carefully chosen to obtain maximum performance.

The aim is to build a DC/DC-converter using silicon components, with a switching frequency which is greater than 2 MHz, having an optimal efficiency and an output power between 15 and 50 W. This set of frequency and power values is very ambitious; it is not easy to switch this amount of power, this fast with normal cooling strategies, using hard-switched silicon components. High frequencies cán be obtained with classic technologies, but the power ratings must then be lowered. Or, the power ratings can, of course, be increased above the value of 50 W chosen for this project, but frequencies must then be decreased. Therefore, soft-switching strategies are chosen to attain previously mentioned output powers at those frequencies. What these strategies are, will be discussed more in detail in the rest of this Chapter. It is the first soft-switched converter, realized in research group Electa.

Furthermore, it is assumed that the converter is supplied from the European low-voltage power grid of 230 V_{rms}, using a rectifier. Hence, a DC-voltage of 325 V appears at the input of the converter. A voltage deviation of ± 10 % is allowed. The output voltage of the converter is 15 V, with a peak-to-peak ripple of 30 mV at an output power of 15 W and of 100 mV when 50 W is delivered. Also, the work aims to maximize the efficiency and also the switching frequency. The specifications are summarized in Table 3.1. In order to compare these specifications with those of other multi-megahertz switched converters (Table 3.2), the output powers and switching frequencies are depicted in Fig. 3.1. Also one example of a converter with GaN HEMTs is included. It can be seen that the minimum specifications of this Chapter, denoted with a circle, are

Table 3.1: Specifications of the converter designed in Chapter 3.

Input voltage	325 V ±10 % DC
Switching frequency	> 2 MHz
Output power	15-50 W
Nominal output voltage	15 V DC
Ripple on output voltage	30 mV_{pp} (at 15 W) - 100 mV_{pp} (at 50 W)

located well within the group of the state-of-the-art multi-megahertz converters, in the lower frequency but higher power zone, indicating that the design is somewhat challenging. References [Xiao 06, Wyk 00, Jaec 93, Alli 79] discuss the hyperbolic nature of the relationship between power and switching frequency. It would be a good idea to plot the power density, that is, the power per unit volume, versus the switching frequency, but unfortunately volume data for the converters of Table 3.2 are not always available.

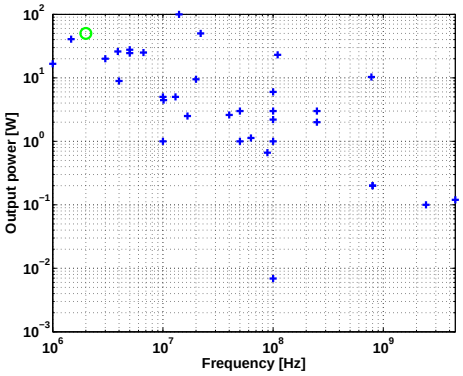


Figure 3.1: Relation between switching frequency and output power of state-of-the-art multi-megahertz DC/DC- or DC/AC-converters. The minimum specifications of the converter designed in this Chapter are denoted by a circle.

3.1.2 Classification of DC/DC-converters

DC/DC-converters can be divided in two groups: switching converters and linear converters (Fig. 3.2). The latter ones use transistors operating in the ohmic region and are equivalent to a resistor. The input and output current are the same and the power which is lost is equal to this current multiplied with the difference of input and output voltage. Therefore, linear converters are not efficient and have large heat losses. However, they have a lower ripple on the output voltage than switching converters and they produce less electromagnetic interference (EMI) [Chet 91, Mamm 01, Eric 01, Moha 02, Rash 04].

Table 3.2: Characteristics of multi-megahertz DC/DC- or DC/AC-converters.

Ref.	**Year**	**Type of converter**	**Technology**	**Output power [W]**	**Switching frequency [MHz]**	**Efficiency [%]**	**Output voltage [V]**	**Output current [A]**	**Volume, or power density**
[Gutm 80]	1980	Class E, single switch	Si	27.64	5	85	5.84	4.7326	NA
				4.46	10.141	68	4.24	1.0095	NA
[Redl 83]	1983	Class E, single switch	Si	40.7	1.47	83.7	22	1.85	NA
[Redl 75]	1986	Class E single switch	Si	100	14	87	20	5	NA
[Bowm 88]	1988	ZVS resonant forward converter, single switch	Si	50	22	78	5	10	0.61 W/cm^3
[Tabi 89]	1989	ZVS QR buck, single switch	Si	25	6.67	80	5	5	NA
				2.5	16.67	72	5	0.5	NA
		ZVS QR flyback, single switch	Si	20	3	70	5	4	NA
				5	13	70	5	1	NA
[Liu 90]	1990	QR boost, single switch	Si	16.65	1	92.4	28.7	0.58	NA
		QR flyback, single switch	Si	24.5	5	83	5	4.9	NA
[Koll 96]	1996	PWM-boost, single switch	GaAs	5	10	85	7	0.72	10.67x0.762x0.1905 mm, 32 W/cm^3
[Ajra 97]	1997	PWM-boost, single switch	GaAs MESFET	2.2	100	69	10	0.22	NA
[Hani 98]	1998	PWM-boost, single switch	AlGaAs/GaAs HEMT	1	10	74	1	1	NA
[Djuk 99]	1999	Class E single switch	Si	0.12	4500	64	3	0.04	140x70x0.508 mm
[Gaye 00]	2000	PWM-buck, single switch	GaAs MESFET	2.6	40	77	5	0.52	NA
[MGay 00]	2000	PWM-Cuk, single switch	GaAs MESFET	1	100	65	-5	0.2	15x15 mm, 1.2 W/cm^3
					50	70	-5	0.2	15x15 mm, 1.2 W/cm^3
[Ajra 01]	2001	PWM-boost, single switch	GaAs MESFET	3	50	80	12	0.25	NA

					100 250	74 60	12 12	0.25 0.25	NA NA
[Suet 03]	2003	Class E single switch and synchr. rectifier	Si	0.2	800	72	4.5	0.0444	0.96x1.6 mm
[Guck 03]	2003	PWM-buck, single switch	SiGe BiCMOS	0.66191	88.7	95.5	3.151	0.2101	0.7x0.215 mm
[Riva 06]	2006	Class E, multiple cells in parallel, each cell having a 6 W rating	Si	6	100	78	5.1	19.6	0.5W/cm^3
[Xiao 06]	2006	Class E, single switch	Si	2	250	46	4.28	0.4673	3x2x0.4 cm, 0.833 W/cm^3
[Pila 07]	2007	Class E Derivative, Resonant Boost Converter (Φ_2-Inverter Combined With Resonant Rectifier), single switch	Si	23	110	87	33	0.697	NA
[Call 12]	2012	Fully-integrated series resonant class DE inverter, single switch	Si	8.9	4	95.7	13.4 peak	1.33 peak	NA
[Li 12]	2012	Differential cascode Class-E Power Amplifier, 12 switches	Si	0.1	2440	43.6	2.4	NA	1.4x1.6 mm
[Hu 12]	2012	Resonant SEPIC converter, single switches	Si	9.5	20	83.6	7	1.36	NA
[Mara 12]	2012	E2 resonant DC/DC converter, single switch for each of the two quadrature legs	GaN HEMTs	10.3	780	72	20	0.5	NA
[Haya 13]	2013	Class E DC/AC Inverter, 2 switches	Si	0.0069	100	65.2	0.585 peak	NA	1.5x0.75 mm

A second class of DC/DC-converters are the switching converters. They use transistors, operated not in the ohmic mode but in the switching mode. While the switch is open, no current can flow through the switch, and while it is closed, the voltage drop across the switch is very small. Because the product of the voltage across the switch and the current through it is equal to the power dissipation in the switch, the losses are smaller than in linear converters, and the efficiency is increased. The resulting waveforms have an AC-characteristic, thus making the insertion of a transformer in the circuit possible, in order to increase or decrease the output voltage.

The switching operation can be 'hard' or 'soft'. Hard-switching DC/DC-converters, also called Pulse-Width Modulated (PWM) DC/DC-converters, take an input DC-voltage and make a high-frequency square wave. The amplitude of this square wave can be controlled with a transformer. A rectifier circuit transforms the square voltage wave into DC, and subsequently, an output filter decreases the ripple of this DC-voltage. The duty ratio, i.e. the percentage of the time that the switch is in its 'on'-state, determines the output voltage. These converter topologies do not allow a very high switching frequency because of the 'hard' switching mechanism:

1. Transistors need to switch off while conducting currents and need to switch on with initially high currents. The switching losses are proportional to the switching frequency, which is thus limited by the cooling mechanism of the converter.

2. The square voltage wave has a broad harmonic spectrum. The transformer in the converter however, is only designed for the fundamental frequency component. Therefore, the higher harmonics lead to increased losses in the transformer.

3. When transistors switch with the 'hard' switching mechanism, the resulting di/dt and dv/dt are large and are the main sources of electromagnetic interference [Chun 98].

4. At higher switching frequencies, waveforms will have shorter rise and fall times. Then, non-ideal components will be more important and will have a negative impact on the operation and performance of the converter. Parasitic inductances of PCB-traces and parasitic capacitances of components will cause crosstalk and will cause signals to 'ring', leading to overvoltages and overcurrents, as is explained in Chapter 4.

In this doctoral work, the purpose is to employ high switching frequencies in converters. In order to attain this, other switching strategies than hard-switching methodologies need to be explored. Soft-switching converters (Fig. 3.2) are converters which alleviate the switching losses using resonant networks, called

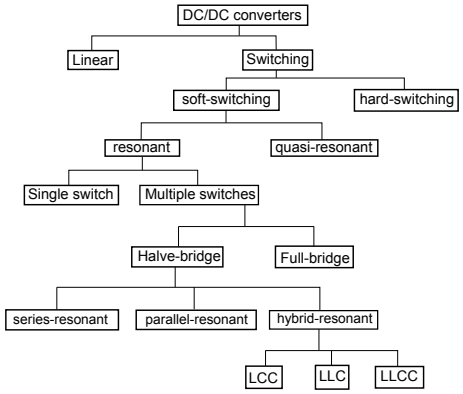


Figure 3.2: Classification of DC/DC-converters.

'tanks', in the power converter, thus facilitating higher switching frequencies. Basically, these resonant tanks create sinusoidal voltage and current waveforms and shape them so that one (or both) of them is zero when the switching occurs, thus leading to zero voltage switching (ZVS) or zero current switching (ZCS). In quasi-resonant converters, there are both resonant and non-resonant operating modi during one switching period, while in resonant converters, there exist only resonant modi. Typically, resonant converters consist of one or more switches which excite a resonant load, while the resonant components are built immediately around the switches in quasi-resonant converters. Resonant converters are sometimes referred to as being 'load-resonant', while quasi-resonant converters are being called 'resonant-switch converters'.

Soft-switching eliminates the switching losses and therefore the need for snubbers [Chet 91, Mamm 01, Wong 95, Hsie 94]. Also, because sinusoidal voltages and currents are created, the dv/dt's and di/dt's remain small, and soft-switching converters therefore produce less EMI than hard-switching converters. Smaller dv/dt's and di/dt's also lead to less ringing, and hence, in a soft-switching converter, the components are subject to less electrical stress. Because only sinusoids are created, the harmonic spectrum of the waveforms in the converter is not so wide and if the converter contains a power transformer, its losses therefore remain small. However, there are also some downsides to soft-switching:

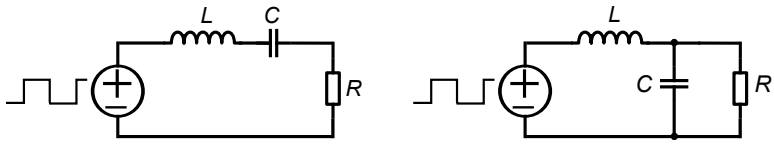
1. The design and implementation is much more difficult than for hard-switching converters.

2. A resonant tank has to be built. Therefore, extra components are necessary. For very high switching frequencies, the parasitic components of the transformers, diodes and transistors can however be used.

3. Sine waves have to be rectified at the output of soft-switching DC/DC-converters, instead of square waves in hard-switching converters. Therefore a larger output filter is required to reach the specifications for the ripple of the output voltage.

Soft-switching converters can be built using a single switch or with multiple switches. Single-switch converters lead to a higher electrical stress on the transistor, while half-bridge converters and especially full-bridge converters are better suited for higher powers. In this Chapter, the input voltage is quite high: 325 V, but the power is maximally 50 W and is not so large; therefore, we opt for a half-bridge topology. An added benefit with respect to a single-switch design is that in a bridge converter, more than one quadrant in the magnetization characteristic of the transformer core material is used, implicating that for a specific apparent power, the volume of the transformer can be decreased [Adai 01].

Finally, a distinction can be made regarding the way the transistor bridge in the converter is loaded. In its most uncomplicated form, the resonant tank only consists of two elements, an inductor L and a capacitor C. If those are in series with each other and with the load, the converter is called a series-resonant converter (Fig. 3.3a). If the frequency is not equal to the resonance frequency, this tank acts like a current source and has a high impedance, seen from the load. The influence of the load R on the current is not too great. If C is in parallel with the load R, the converter is a parallel-resonant converter (Fig. 3.3b). The behaviour of the tank is that of a voltage source, and the load R does not influence its own voltage too much. For frequencies not too close to the resonance frequency, the tank has a low impedance as seen from the load. If multiple resonant components are used in the tank, one can use them in multiple combinations. With three components C, L_s and L_p, a hybrid version, also called a series-parallel-resonant converter, is possible [Stei 88, Laza 01] (Fig. 3.4). This circuit combines the advantages of a series converter with those of a parallel converter. With more than three components, even more degrees of freedom are available to shape the input impedance of the tank circuit. Higher efficiencies are possible and these designs are called multiresonant converters [Chak 02, Yang 03].



(a) Series-resonant converter. (b) Parallel-resonant converter.

Figure 3.3: Tanks of a series- and of a parallel-resonant converter.

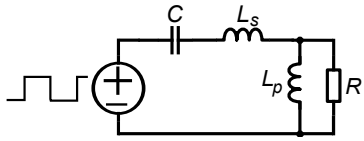


Figure 3.4: Hybrid resonant converter (type LLC).

3.1.3 Condition for zero voltage switching

Switching on occurs with zero voltage (ZVS) in the half-bridge circuit of Fig. 3.6 when the impedance Z, connected to the half-bridge is inductive. The reason for this is depicted in Fig. 3.5a. At time t_0, switch S_2 turns on. Before t_0, there was a time interval $t_{dead,1}$, called dead time, where both switches S_1 and S_2 were open to avoid a short circuit. During the dead time interval $t_{dead,1}$ the current i will first flow through the drain-to-source capacitance of S_2 discharging it, and when there is some more time left, i will flow through the antiparallel diode D_2. If $t_{dead,1}$ is long enough and i is high enough, the drain-to-source capacitance of S_2 will be discharged completely and S_2 can turn on at zero volts. This is only possible with inductive currents.

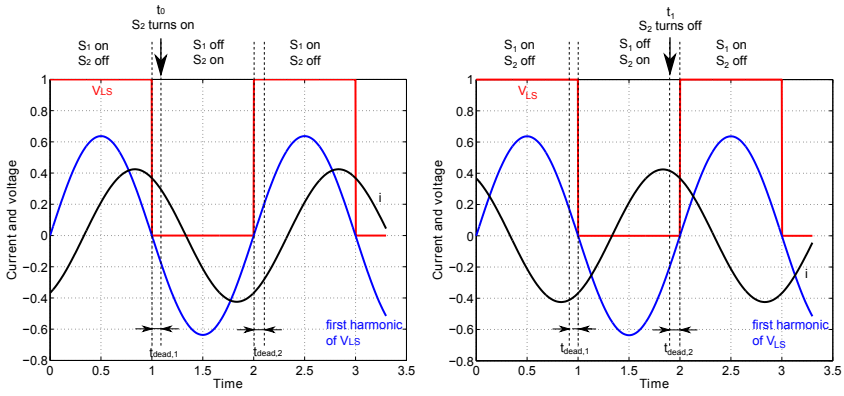
However, capacitive currents are useful too. Referring to Fig. 3.5b, for such currents, it can be seen that the current i is positive at time t_1 when S_2 turns off. This means that i flows through the antiparallel diode D_2 of S_2 and that S_2 switches off without current (ZCS).

We can conclude:

$$\boxed{\begin{array}{lcl} \text{turn-on} = \text{ZVS} & \Rightarrow & Z = \text{inductive} \\ \text{turn-off} = \text{ZCS} & \Rightarrow & Z = \text{capacitive} \end{array}}$$

These are actually **necessary** conditions for zero voltage or zero current switching, but **not sufficient** conditions. An inductive resonant tank current discharges the output capacitor of the MOSFETs during the dead time period, but there will be only zero voltage switching if the current is high enough or the dead time period is long enough to discharge the output capacitor completely before the MOSFET turns on again.

In Fig. 3.8, the gate-to-source signals applied to the low-side and high-side MOSFETs in a half-bridge are shown. The low-side MOSFET turns off, while the high-side MOSFET turns on, a dead time t_{dead} later. The voltage across the low-side MOSFET, V_{LS}, is also depicted. It typically has an S-shape because the output capacitances of MOSFETS are large at a low voltage and decrease rapidly with increasing voltage. So, first, the output capacitor of the low-side MOSFET is charged by a part of the resonant tank current $i(t)$, and because it is discharged at first, its output capacitance is large and the voltage



(a) Inductive current - ZVS.

(b) Capacitive current - ZCS.

Figure 3.5: Deriving a condition for soft-switching.

across it will rise rather slowly. Then, after the initial part with the small slope, an steep increase in the voltage V_{LS} can be observed, because the output capacitance of the low-side MOSFET assumes a low value when the voltage becomes sufficiently high. Next, the voltage V_{LS} increases again slowly over time, because the resonant tank current is also used to discharge the high-side MOSFET, of which the output capacitance has a large value when the voltage across it becomes low.

The voltage across the low-side MOSFET can be decomposed in its Fourier components. If the rising behaviour and the falling behaviour of V_{LS} are symmetrical, and if the first harmonic of V_{LS} is represented with a sine function: $V_{LS}^{FHA} \propto \sin(\omega t)$, then the zero of the time is located where V_{LS} has half the value of the supply voltage of a half-bridge resonant converter. Also, the current in the resonant tank is then:

$$i(t) = \widehat{I} \sin(\omega t + \phi) \tag{3.1}$$

If the two MOSFETs in the half-bridge are the same, the negative resonant tank current is used during the dead time period to charge the low-side MOSFET's output capacitor $C_{oss} \approx C_{ds} + C_{gd}$ from zero voltage to V_{in} and to discharge the high-side MOSFET's output capacitor from V_{in} to zero volts. This can be observed in Fig 3.7, where the case for a positive current i is shown. It is seen that the tank current flows through the two output capacitors of the MOSFETs, and that the high-side MOSFET is charged and that the low-side MOSFET is discharged in parallel.

In the datasheet of MOSFETs the output capacitance is given as a small signal value and usually a figure depicting the strong voltage-dependency is given.

$$C_{oss} = \frac{dQ_{oss}}{dV_{ds}} \tag{3.2}$$

V_{ds} is the drain-to-source voltage across the MOSFET. We have, with Q the sum of the charges that can be stored in the output capacitors of the low-side and the high-side MOSFETs:

$$Q = \int_0^{V_{in}} \left(C_{oss}(V_{ds}) + C_{oss}(V_{in} - V_{ds})\right) dV_{ds} = -\int_{-t_{rise}/2}^{t_{rise}/2} i(t)dt \tag{3.3}$$

However, by substitution and reversing the limits of the integration, the first integral can be rewritten as:

$$Q = 2\int_0^{V_{in}} C_{oss} dV_{ds} \tag{3.4}$$

We thus have:

$$\begin{aligned} \frac{Q}{2} = \int_0^{V_{in}} C_{oss} dV_{ds} &= -\frac{1}{2\omega}\widehat{I}\left[-\cos(\omega t + \phi)\right]_{-t_{rise}/2}^{t_{rise}/2} \\ &= \frac{\widehat{I}}{2\omega}\left[\cos(\frac{\omega t_{rise}}{2} + \phi) - \cos(\frac{-\omega t_{rise}}{2} + \phi)\right] \\ &= \frac{-\widehat{I}}{\omega}\sin(\phi)\sin\frac{\omega t_{rise}}{2} \end{aligned} \tag{3.5}$$

From this equation, the rise time of V_{LS} can be determined, if the amplitude and phase of the resonant tank current are known:

$$t_{rise} = \frac{2}{\omega}\arcsin\left(\frac{-Q\omega}{2\widehat{I}\sin(\phi)}\right) \tag{3.6}$$

In this equation, Q is obtained from the MOSFET's datasheet by integrating C_{oss} over the voltage from 0 V to V_{in}. The moment where the tank current crosses the time-axis is t_1 and can be found by equating $\omega t_1 + \phi$ to zero. Thus:

$$t_1 = \frac{-\phi}{\omega} \tag{3.7}$$

There are two **necessary and sufficient** conditions for zero voltage switching with an inductive tank current. They are:

1. $t_{dead} \geq t_{rise}$, in order to fully charge the low-side output capacitor and discharge the high-side output capacitor before the latter switches on. Thus, we have:

$$\boxed{t_{dead} \geq t_{rise} = \frac{2}{\omega} \arcsin\left(\frac{-Q\omega}{2\widehat{I}\sin(\phi)}\right)} \tag{3.8}$$

2. In order not to charge the high-side capacitor with a positive tank current before it switches on, or discharge the low-side capacitor with this positive current after it is already fully charged, a second condition must be demanded: $t_1 \geq t_{dead} - t_{rise}/2$. We thus have:

$$\boxed{t_{dead} \leq t_1 + \frac{t_{rise}}{2}} \tag{3.9}$$

These two conditions give an upper and lower bound on the dead time, in order for ZVS to be achieved, when the frequency and tank current are known. The formulas are a contribution of this work.

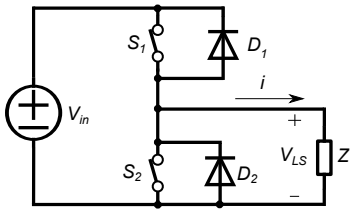


Figure 3.6: Explanation of ZVS.

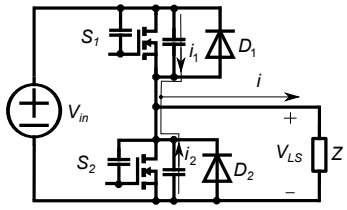


Figure 3.7: Charging and discharging the two output capacitances in parallel.

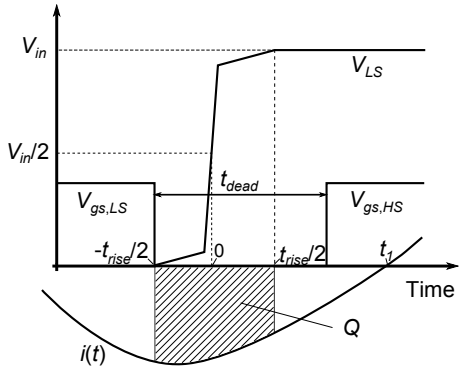


Figure 3.8: Deriving a necessary and sufficient condition for ZVS at turn-on.

3.1.4 Choice of switching components

MOSFETs are unipolar devices and therefore faster than bipolar components such as Insulated Gate Bipolar Transistors (IGBTs) [Moha 02]. Hence, for the project of this work, focussing on fast converters, MOSFETs are chosen. MOSFETs are best suited to be applied in ZVS-converters, while IGBTs are best suited for ZCS-converters. The reasons for this will be now given. The switching losses of MOSFETs consist of three terms ([Xion 09], formula (1) and (3)), one proportional to the turn-on gate charge and drain voltage V_{DD}, one-proportional to the turn-off gate charge and the drain voltage V_{DD}, and the third proportional to the square of the drain voltage V_{DD}^2.This third contribution to the switching losses is the energy, stored in the drain-to-source capacitance during the off-time, which is dissipated in the on-resistance when the transistor switches on again. However, when the transistor switches on at zero voltage, this third term, being proportional to V_{DD}^2, becomes zero. Also, the first contribution, proportional to the turn-on gate charge, becomes very small, because V_{DD} is very small and the Miller effect is furthermore almost absent causing the turn-on gate charge to decrease dramatically.

An n-channel IGBT on the other hand, can be modelled as a pnp-bipolar transistor, that is driven by an n-MOS [Moha 02] (Fig. 3.9). When it turns off, a positive base current is needed to stop the conduction process of the pnp-transistor. Because of the structure of the IGBT, this positive current, which is directed towards the base, cannot flow immediately during the turn-off process.

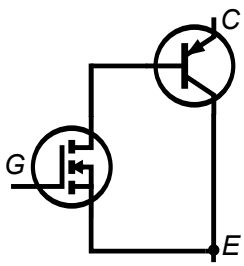


Figure 3.9: IGBT: model.

Hence, during turn-off, the charge carriers will recombinate naturally while the conduction current will keep on flowing for a while. It will therefore take a while for the collector current to become zero during the turn-off transient. The collector current has a "tailing" behaviour. This slow decrease of the collector current increases the switching losses. Therefore, ZCS is very appropriate when IGBTs are used in a converter.

3.2 Resonant converters

In this Section, a literature overview will be given of currently used resonant converter topologies and their advantages and disadvantages.

3.2.1 Series-resonant converters

A series-resonant converter has a resonant inductor L_r and capacitor C_r in series with each other and in series with the load (Fig. 3.10).

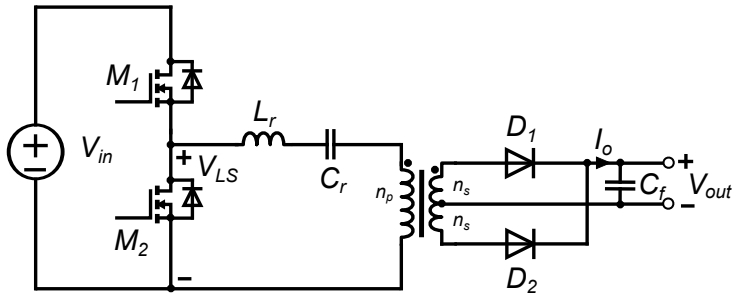


Figure 3.10: Series-resonant converter.

The resonant network is called a tank. The resonant tank forms a voltage divider with the rectifier and load resistance, so that the amplification factor is always smaller than 1. Changing the switching frequency changes the impedance of the resonant tank. Therefore, control of the frequency allows regulation of the power which flows towards the load.

The behaviour of this tank can be studied using an AC-analysis. The series-resonant converter uses a capacitive output filter C_f and feeds the rectifier with an AC-current source [Stei 88]. The half-bridge applies a voltage which is a square wave, to the resonant tank. This tank filters the higher harmonic components of the voltage and that is why only a sinusoidal current is allowed to flow through the tank. At the secondary side of the transformer, a voltage appears which is a square wave because the capacitive output filter tends to keep the output voltage constant. It will now be shown that the rectifier and load can be represented by an equivalent resistance. The equivalent resistance seen from the resonant tank, can be calculated as follows (Fig. 3.11).

The output current I_{load}, flowing through the load resistance, is the average of the rectified current flowing out of the diode rectifier. This rectified current is equal to $|I_{AC}(t)|$:

$$I_{load} = \langle \left| \widehat{I}_{AC} \sin(\omega t) \right| \rangle = \widehat{I}_{AC} \frac{1}{\pi} \int_0^{\pi} \sin(\omega t) d(\omega t) = \frac{2\widehat{I}_{AC}}{\pi} \tag{3.10}$$

From this, it follows that:

$$I_{AC}(t) = \frac{\pi I_{load}}{2} \sin(\omega t) \tag{3.11}$$

The square wave V_s appearing over the secondary coil of the transformer varies between V_{out} and $-V_{out}$, and therefore has an amplitude equal to V_{out}. We

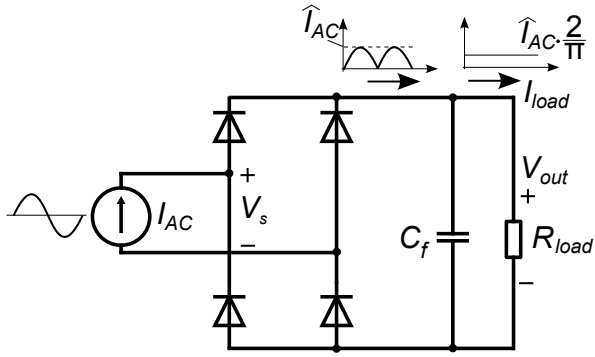


Figure 3.11: Calculation of the equivalent AC-resistance of a series-resonant converter.

make a first-harmonic approximation (FHA) [Stei 88], assuming that only the fundamental component contributes to the power transfer, and the fundamental component of V_s is therefore:

$$V_s^{FHA} = \frac{4V_{out}}{\pi}\sin(\omega t) \tag{3.12}$$

The current and voltage at the input of the rectifier are in phase, because the voltage drop across the diodes of the rectifier is assumed to be zero. The equivalent load resistance seen from the secondaries of the transformer is then equal to:

$$R_{AC}^{sec} = \frac{V_s^{FHA}}{I_{AC}} = \frac{4V_{out}/\pi}{\pi I_{load}/2} = \frac{8}{\pi^2}\frac{V_{out}}{I_{load}} = \frac{8}{\pi^2}R_{load} \tag{3.13}$$

The equivalent resistance of the rectifier network connected to the load resistance, as seen from the input of the transformer is then:

$$R_{AC}^{prim} = \frac{8n^2}{\pi^2}R_{load} \tag{3.14}$$

with $n = n_p/n_s$ the transformation ratio. The AC-equivalent circuit is shown in Fig. 3.12. All the quantities are referred to the primary side. The amplification factor M can now be calculated. It is the ratio of the amplitude of the fundamental component of the voltage at the output of the resonant tank to the amplitude of the fundamental component of the voltage at the input of the resonant tank. The voltage at the input of the resonant tank (Fig. 3.10) is V_{LS}, which is a square wave voltage between V_{in} and 0. The amplitude of the fundamental component is:

$$\left|V_{LS}^{FHA}\right| = \frac{4}{\pi}\frac{V_{in}}{2} \tag{3.15}$$

Therefore, the amplification factor of the resonant tank is

$$M = \left| \frac{nV_s^{FHA}}{V_{LS}^{FHA}} \right| = \frac{n\frac{4V_{out}}{\pi}}{\frac{4}{\pi}\frac{V_{in}}{2}} = \frac{2nV_{out}}{V_{in}} \tag{3.16}$$

When the switching frequency is equal to the resonance frequency of the tank, the amplification is equal to 1. The resonance frequency is:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{3.17}$$

The quality factor of the resonant tank is:

$$Q = \frac{\sqrt{L_r/C_r}}{R_{AC}^{prim}} \tag{3.18}$$

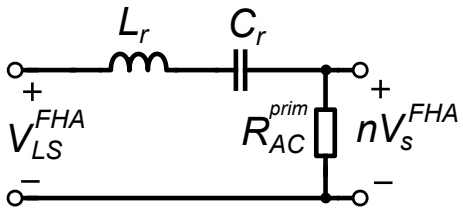


Figure 3.12: AC-equivalent circuit of the series-resonant converter.

In Fig. 3.13, the amplification curve is shown in function of the frequency for a series-resonant converter with:

$C_r = 350$ pF	$L_r = 17$ μH
$V_{in} = 325$ V ± 10 %	$V_{out} = 15$ V
$n = n_p/n_s = 9$	$R_{load} = 4.5 - 15$ Ω

The maximum and minimum load resistances are determined so that, at 15 V, the output power is equal to respectively 15 and 50 W. With the listed values of C_r and L_r, the resonance frequency is $1/(2\pi\sqrt{L_r C_r}) \approx 2$ MHz. It is advantageous to operate the converter in the ZVS mode when using MOSFETs as switching components (cf. Section 3.1.4). From Section 3.1.3, we know that ZVS can be achieved if the input impedance of the resonant tank is inductive. This is a necessary condition for ZVS; however, the condition is not sufficient. From the phase characteristic (Fig. 3.14), it can be seen that this inductive behaviour is attained for frequencies above the resonance frequency. In Fig. 3.13, the inductive region, where ZVS can be achieved, is coloured light grey, and the capacitive region, where ZCS can occur, is coloured dark grey. Two magnification curves are plotted thicker: the curves of minimum and maximum load ($R_{load} =$

15 Ω and 4.5 Ω). Two horizontal lines correspond to the minimum input voltage $325 \cdot 0.9 = 292.5$ V and to the maximum input voltage $325 \cdot 1.1 = 357.5$ V. The two vertical lines give the control area: this is the interval in which the switching frequency should vary in order to achieve an output voltage of 15 V, for input voltages between 292.5 and 357.5 V, when the load varies between 4.5 and 15 Ω.

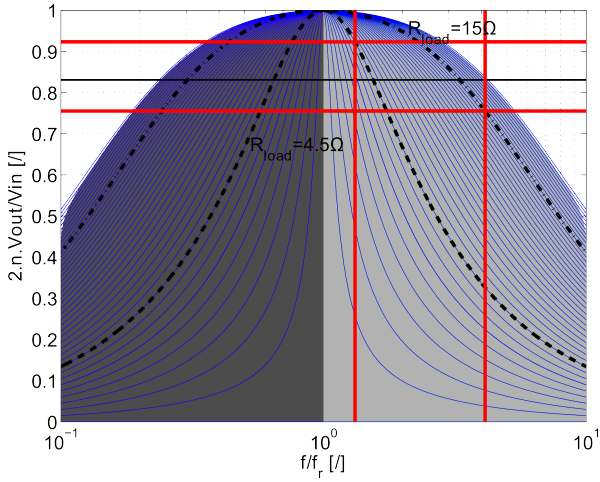


Figure 3.13: Amplification factor of a series-resonant converter; light grey = possible ZVS-region, dark grey = possible ZCS-region.

Some remarks can be drawn from these Figures, regarding the advantages and disadvantages of a series-resonant converter:

- As can be seen from the magnification characteristic, the frequency has to be very high in order to control the output voltage for low loads (high output resistances). Thus, the series-resonant converter is not suited to use for low loads [Chak 02] [Shah 90].
- As can be seen from the impedance characteristic, the current in the resonant tank increases when the load increases. The reason for this is that the absolute value of the input impedance of the tank increases with the load resistance. This leads to a good efficiency at both low and high loads [Shah 90] [Hsie 07].
- Because in the resonant tank, the inductor is in series with the load, the current in the tank will be limited in case of a short circuit at the load [Shah 90] [Hsie 07].

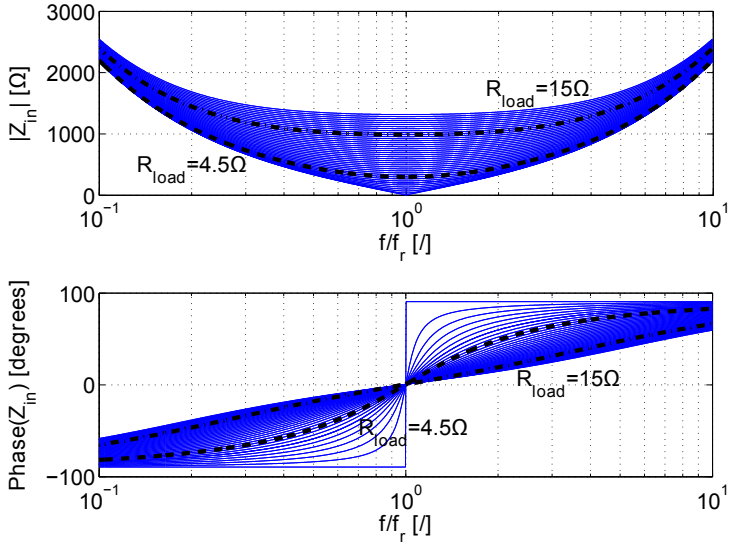


Figure 3.14: Amplitude and phase of the impedance, seen at the input of the resonant tank in a series-resonant converter.

- The current ripple at the output is higher than for other types of resonant converters, because the output filter doesn't contain an inductance [Shah 90].
- A negative point is that the more the frequency differs from the resonance frequency, the phase difference between current and voltage increases. From Fig. 3.5a, it can be seen that when we want to turn S_1 off, a higher current should be switched off, resulting in higher switching losses for the MOSFET if there is a non-zero voltage across. Furthermore, the more the switching frequency and the resonance frequency differ, the more energy is sent to the input capacitors during the dead time and the time period that the high-side diode conducts. This means that the size of the input capacitors increases.
- When the resonant capacitor increases, the resonance frequency decreases. When the converter is operated at the same frequency, the magnitude of the input impedance of the tank increases. This means that the resonant tank current decreases and that less current is available to discharge the output capacitor of the MOSFET during the dead-time. Hence, when C_r increases, zero voltage switching can be lost, especially at low load. This occurs for instance when in the design of the converter, the drain-to-source capacitances of the MOSFETs are not taken into account, or are of the order of magnitude ($\propto$ 100 pF) of the external C_r. The total resonant capacitance then increases, and while in the (faulty) design there still

is ZVS, this is not true anymore in reality. It can be shown that the series-resonant converter is the resonant converter which is the most prone to this phenomenon [Saba 96].

3.2.2 Parallel-resonant converters

A parallel-resonant converter has a capacitor C_r in parallel with the load and a resonant inductor L_r in series with this parallel circuit (Fig. 3.15). This converter is also called a series-resonant converter with a parallel load.

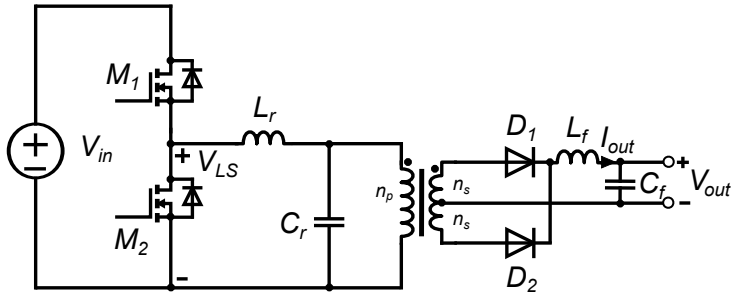


Figure 3.15: Parallel-resonant converter.

Because there is a capacitor in parallel with the primary side of the transformer, the output filter should have an inductor L_f. If this inductor is not there and the output filter would only exist of a capacitor C_f, at the primary side of the transformer there would be a voltage varying between nV_{out} and $-nV_{out}$. The parallel resonant capacitor C_r does not allow the voltage to vary instantaneously however, so an inductor in the output filter is needed.

The behaviour of this tank can again be studied using an AC-analysis. The current I_{out} through the filter inductor L_f can be assumed constant. Therefore, the current at the input of the diodes D_1 and D_2 is a square wave, varying between I_{out} and $-I_{out}$. However, the voltage across the resonant capacitor C_r is sinusoidal as the resonant tank acts like a filter for the square wave voltage pulse which is applied to the tank by the half-bridge. The current in the secondary coil of the transformer is a square wave between I_{out} and $-I_{out}$ and has a fundamental component:

$$I_s^{FHA}(t) = \frac{4I_{out}}{\pi}\sin(\omega t) \tag{3.19}$$

The secondary voltage V_s is sinusoidal and when it is rectified and then averaged, one obtains the output voltage V_{out}. Denote the amplitude of the secondary voltage by $\widehat{V}_{AC}$:

$$V_{out} = \langle|\widehat{V}_{AC}\sin(\omega t)|\rangle = \frac{2\widehat{V}_{AC}}{\pi} \tag{3.20}$$

From this, it follows that:

$$V_s(t) = \frac{\pi V_{out}}{2} \sin(\omega t) \tag{3.21}$$

The current at the secondary side and the voltage are in phase, as the voltage drop across the output diodes is zero. The equivalent load resistance seen from the secondaries of the transformer is thus equal to:

$$R_{AC}^{sec} = \frac{V_s}{I_s^{FHA}} = \frac{\pi V_{out}/2}{4I_{out}/\pi} = \frac{\pi^2}{8}\frac{V_{out}}{I_{out}} = \frac{\pi^2}{8} R_{load} \tag{3.22}$$

The equivalent resistance of the rectifier network connected to the load resistance, as seen from the input of the transformer is then:

$$R_{AC}^{prim} = \frac{n^2\pi^2}{8} R_{load} \tag{3.23}$$

with $n = n_p/n_s$ the transformation ratio. The AC-equivalent circuit is shown in Fig. 3.16. All quantities are referred to the primary side. The amplification factor M of the resonant tank can again be calculated. It is the ratio of the fundamental component of the voltage at the output of the resonant tank to the fundamental component of the voltage at the input of the resonant tank. The voltage at the input of the resonant tank (Fig. 3.15) is V_{LS}, which is a square wave voltage between V_{in} and 0. The amplitude of the fundamental component is:

$$\left|V_{LS}^{FHA}\right| = \frac{4}{\pi}\frac{V_{in}}{2} \tag{3.24}$$

Therefore, the amplification factor is

$$M = \left|\frac{nV_s}{V_{LS}^{FHA}}\right| = \frac{n\frac{\pi V_{out}}{2}}{\frac{4}{\pi}\frac{V_{in}}{2}} = \frac{n\pi^2 V_{out}}{4V_{in}} \tag{3.25}$$

The resonance frequency is:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{3.26}$$

The quality factor of the resonant tank is [Stei 88]:

$$Q = \frac{R_{AC}^{prim}}{\sqrt{L_r/C_r}} \tag{3.27}$$

In Fig. 3.17, the amplification curve is shown in function of the frequency for a parallel-resonant converter with:

$C_r = 350$ pF	$L_r = 17$ μH
$V_{in} = 325$ V ± 10 %	$V_{out} = 15$ V
$n = n_p/n_s = \lceil 325/(2 \cdot 15) \rceil = 11$	$R_{load} = 4.5 - 15$ Ω

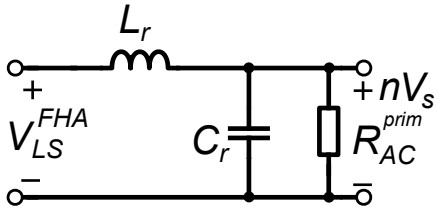


Figure 3.16: AC-equivalent circuit of the parallel-resonant converter.

The maximum and minimum load resistances are determined so that, at 15 V, the output power is equal to respectively 15 and 50 W. With the listed values of C_r and L_r, the resonance frequency is $1/(2\pi\sqrt{L_r C_r}) \approx 2$ MHz. From the phase characteristic (Fig. 3.18), it can be determined for which frequencies the tank is inductive, and therefore if ZVS can be achieved. In Fig. 3.17, the inductive region, where ZVS can be achieved, is coloured light grey and the capacitive region, where ZCS can occur, is coloured dark grey. The inductive nature of the resonant tank is a necessary condition for ZVS; however, the condition is not sufficient. Notice that the border between the possible ZCS- and the ZVS-region is not located on the maximum of the amplification curves. Two magnification curves are plotted thicker: the curves of minimum and maximum load ($R_{load} = 15\ \Omega$ and $4.5\ \Omega$). Two horizontal lines correspond to the minimum input voltage $325 \cdot 0.9 = 292.5$ V and to the maximum input voltage $325 \cdot 1.1 = 357.5$ V. The two vertical lines give the control area: the interval in which the switching frequency should vary in order to achieve an output voltage of 15 V, for input voltages between 292.5 and 357.5 V, when the load varies between 4.5 and 15 Ω.

The parallel-resonant converter has a few advantages:

- In comparison with the series-resonant converter, the frequency-control-interval is much smaller.
- When the load suddenly drops or rises, the parallel-resonant converter performs better than the series-resonant converter, because in order to regulate the output voltage, a smaller frequency excursion is needed, as compared to the series converter.
- The parallel-resonant converter is a lot less sensitive to the presence of the output capacitance of the switching devices in the half-bridge, as compared to the series converter. This is empirically shown in [Saba 96].

But the converter also has some disadvantages:

- When the load is a short-circuit, the resonant capacitance C_r will also be short-circuited, causing a greater short-circuit current than in a series

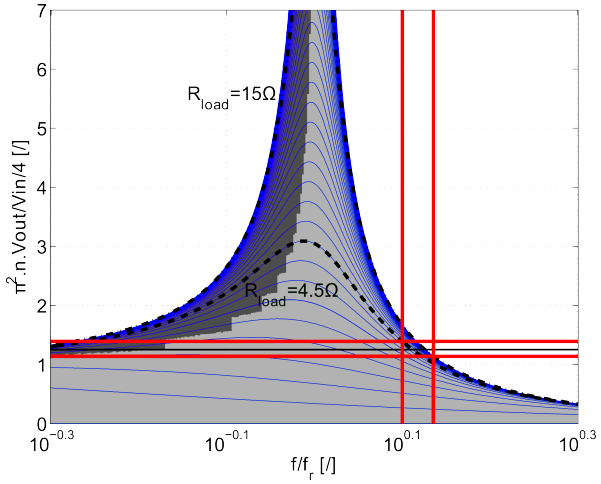


Figure 3.17: Amplification factor of the resonant tank of a parallel-resonant converter; light grey = possible ZVS-region, dark grey = possible ZCS-region.

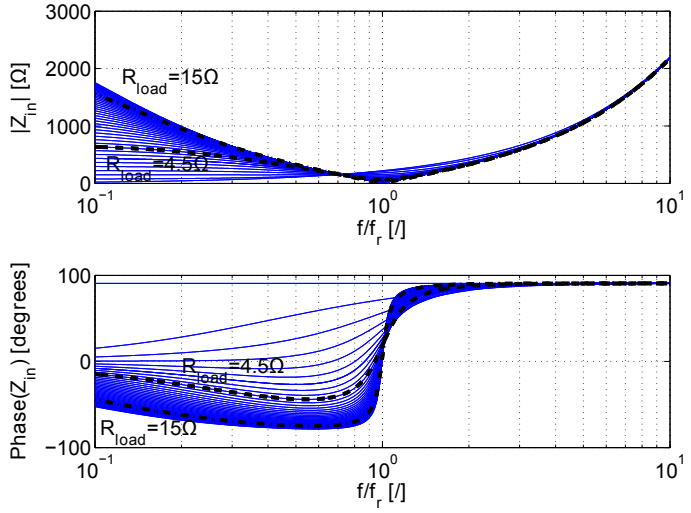


Figure 3.18: Amplitude and phase of the impedance, seen at the input of the resonant tank in a parallel-resonant converter.

converter with comparable resonant components. Therefore, an additional overload-protection is necessary [Shah 90].

- The circulating energy in the resonant tank is higher than in a series converter, and is almost independent of the load [Chak 02]. The reason for this is the presence of the resonant capacitance C_r, placed in parallel with the load. Even at a low load (high load resistance R_{load}), the half-bridge sees a relatively small impedance, resulting in a high circulation current [Yang 03].

3.2.3 Series-parallel-resonant converters, type LCC

A series-parallel-resonant converter of the LCC-type is depicted in Fig. 3.19. There are three resonant components in the tank. This increases the complexity of the tank and of the converter analysis, but at the same time, the advantages of the series- and of the parallel-resonant converter can be combined [Chen 06].

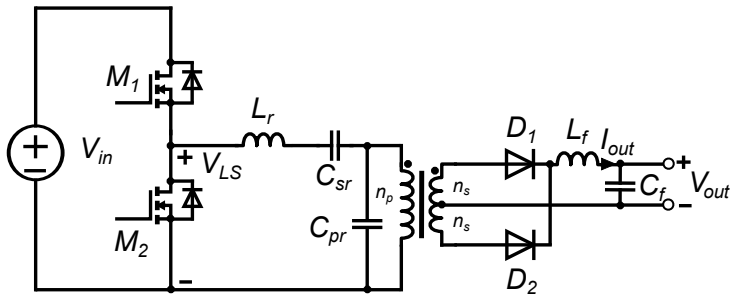


Figure 3.19: Series-parallel-resonant converter, type LCC.

In this type of tank, two resonance frequencies are present [Stei 88]:

$$f_{r,1} = \frac{1}{2\pi\sqrt{C_{sr}L_r}} = f_r \tag{3.28}$$

$$f_{r,3} = \frac{1}{2\pi\sqrt{\frac{L_r C_{sr} C_{pr}}{C_{pr}+C_{sr}}}} \tag{3.29}$$

with $f_{r,3} > f_{r,1}$ because $\frac{C_{sr}C_{pr}}{C_{pr}+C_{sr}} < \min\{C_{pr}, C_{sr}\}$. The second resonance frequency occurs due to the resonance of C_{sr} and C_{pr} in series with each other, together with L_r. Because of the presence of the capacitance C_{pr} in parallel with the transformer, an inductor L_f is needed in the output filter, just like in the case of a parallel-resonant converter.

This hybrid type of converter combines the advantages of both the series- and the parallel-resonant converter [Chen 06]:

- Like in the series-resonant converter, because the load is in series with the tank inductor L_r and the resonant capacitor C_{sr}, the circulation current in the tank will be limited.
- Just like in the case of the parallel-resonant converter, because of the presence of the parallel resonant capacitor C_{pr}, the converter is able to regulate the output voltage well at no-load [Yang 03].
- The efficiency at both high and low loads is good [Shah 90], as is the case of series converters.
- The LCC-converter can deal with short circuits in the load, as can a series converter.

The behaviour of this tank can again be studied using an AC-analysis (Fig. 3.20). The derivation of the amplification factor M of the resonant tank and the equivalent output resistance is analogous to the parallel-resonant converter, because the LCC-converter also has an inductor in the output filter:

$$R_{AC}^{prim} = \frac{\pi^2 n^2}{8} R_{load} \tag{3.30}$$

$$M = \frac{n\pi^2 V_{out}}{4V_{in}} \tag{3.31}$$

The quality factor of the resonant tank is [Stei 88]:

$$Q = \frac{\sqrt{L_r/C_{sr}}}{R_{AC}^{prim}} \tag{3.32}$$

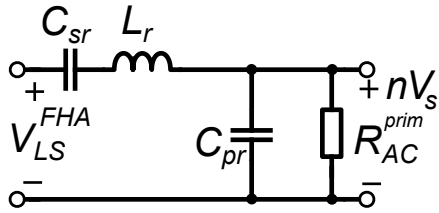


Figure 3.20: AC-equivalent circuit of the LCC-converter.

In Fig. 3.21, the amplification curve is shown in function of the frequency for an LCC-converter with:

$C_{sr} = 350$ pF	$L_r = 17$ μH
$C_{pr} = 100$ pF	
$V_{in} = 325$ V ± 10 %	$V_{out} = 15$ V
$n = n_p/n_s = \lceil 325/(2 \cdot 15) \rceil = 11$	$R_{load} = 4.5 - 15$ Ω

With the listed values of C_{sr} and L_r, the first resonance frequency is $f_{r,1} = 1/(2\pi\sqrt{L_r C_{sr}}) \approx 2$ MHz. From the phase characteristic (Fig. 3.22), it can be determined for which frequencies the tank is inductive, and therefore where ZVS can be achieved. In Fig. 3.21, the inductive region, where ZVS can be achieved, is coloured light grey, and the capacitive region, where ZCS can occur, is coloured dark grey. Notice that the border between the possible ZCS- and the ZVS-region is not located on the maximum of the amplification curves. Actually, the border between the two regions should be more smooth. The fact that it is not in the Figure, is due to a too coarse numerical interpolation. Also notice that the inductive nature of the resonant tank is a necessary condition for ZVS; however, the condition is not sufficient. Two magnification curves are plotted thicker: the curves of minimum and maximum load ($R_{load} = 15\ \Omega$ and $4.5\ \Omega$). Two horizontal lines correspond to the minimum input voltage of $325 \cdot 0.9 = 292.5$ V and to the maximum input voltage of $325 \cdot 1.1 = 357.5$ V. The two vertical lines give the frequency control region.

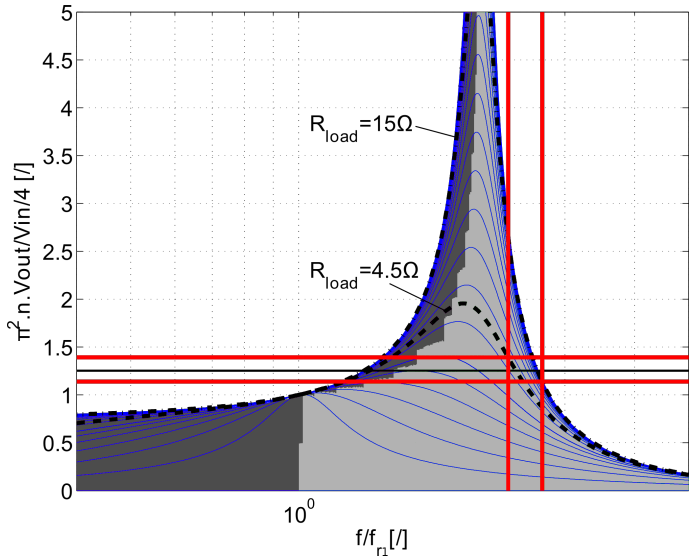


Figure 3.21: Amplification factor of the resonant tank of an LCC-converter; light grey = possible ZVS-region, dark grey = possible ZCS-region.

The possible ZVS-region is mainly located at frequencies higher than the first resonance frequency $f_{r,1}$. One operates the LCC-converter therefore at frequencies higher than the second resonance frequency $f_{r,3}$, to ensure ZVS. At a higher input voltage ($M \downarrow$), the operating point will move to the right, and the switching frequency needs to increase. Considering the phase characteristic of the tank input impedance, it can be seen that then the phase difference between voltage and current increases, leading to a higher circulating current

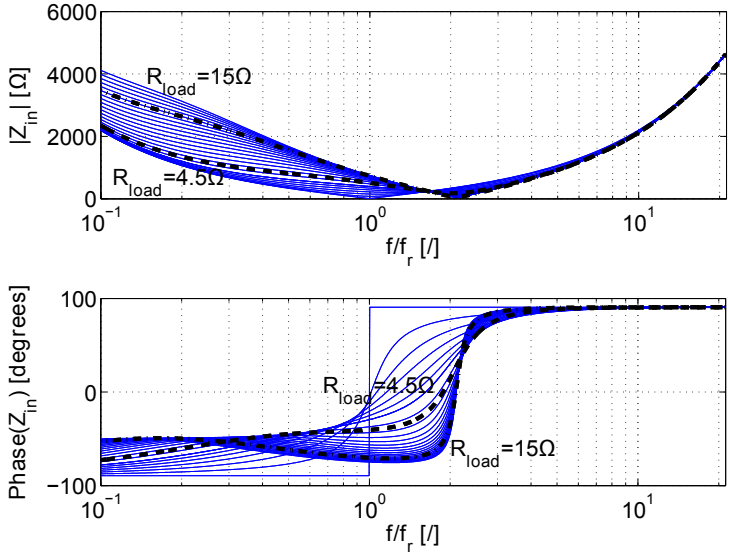


Figure 3.22: Amplitude and phase of the impedance, seen at the input of the resonant tank in an LCC-converter.

and therefore higher switching losses in the MOSFETs if there is a non-zero voltage across them.

In comparison with the LLC-converter, the needed operating frequencies are greater. The reason for this is that one needs frequencies higher than $f_{r,3}$ to ensure ZVS in an LCC-converter. Using frequencies close to the first resonance frequency $f_{r,1}$ can circumvent this problem. However, then, ZVS can only be guaranteed at very high loads. Close to the first resonance frequency, ZVS can be lost at lower loads (higher load resistances), and operating the converter around $f_{r,1}$ is therefore not recommended.

3.2.4 Series-parallel-resonant converters, type LLC

A series-parallel-resonant converter of the LLC-type is depicted in Fig. 3.23.

In this type of tank, two resonance frequencies are present [Fair 12]:

$$f_{r,1} = \frac{1}{2\pi\sqrt{C_r L_{sr}}} = f_r \tag{3.33}$$

$$f_{r,2} = \frac{1}{2\pi\sqrt{C_r (L_{sr} + L_{pr})}} \tag{3.34}$$

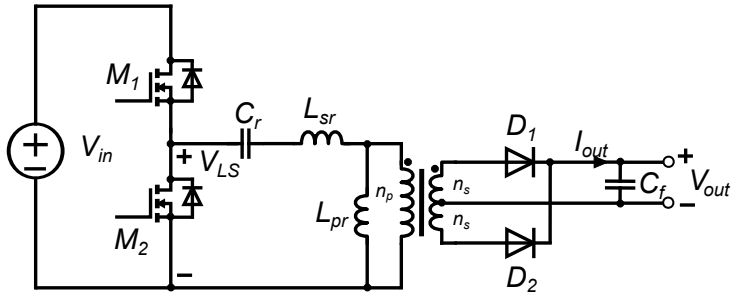


Figure 3.23: Series-parallel-resonant converter, type LLC.

with $f_{r,2} < f_{r,1}$. The behaviour of this tank can again be studied using an AC-analysis (Fig. 3.24). The derivation of the amplification factor M of the resonant tank and the equivalent output resistance is analogous to the series-resonant converter, because the LLC-converter also only has a capacitor in the output filter:

$$R_{AC}^{prim} = \frac{8n^2}{\pi^2} R_{load} \tag{3.35}$$

$$M = \frac{2nV_{out}}{V_{in}} \tag{3.36}$$

The quality factor of the resonant tank is [Fair 12]:

$$Q = \frac{\sqrt{L_{sr}/C_r}}{R_{AC}^{prim}} \tag{3.37}$$

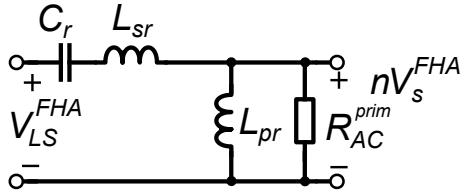


Figure 3.24: AC-equivalent circuit of the LLC-converter.

In Fig. 3.25, the amplification curve is shown in function of the frequency for an LLC-converter with:

$C_{sr} = 350$ pF	$L_r = 17$ μH
$L_{pr} = 45$ μH	
$V_{in} = 325$ V ± 10 %	$V_{out} = 15$ V
$n = n_p/n_s = \lceil 325/15 \rceil = 11$	$R_{load} = 4.5 - 15$ Ω

With the listed values of C_r and L_{sr}, the first resonance frequency is $f_{r,1} = 1/(2\pi\sqrt{L_{sr}C_r}) \approx 2$ MHz. From the phase characteristic (Fig. 3.26), it can be determined for which frequencies the tank is inductive and therefore where ZVS can be achieved. In Fig. 3.25, the inductive region, where ZVS can be achieved, is coloured light grey, and the capacitive region, where ZCS can occur, is coloured dark grey. Notice that the border between the ZCS- and the ZVS-region is not located on the maximum of the amplification curves. Actually, the border between the two regions should be more smooth. The fact that it is not in the Figure, is due to a too coarse numerical interpolation. Also notice that the inductive nature of the resonant tank is a necessary condition for ZVS; however, the condition is not sufficient. Two magnification curves are plotted thicker: the curves of minimum and maximum load ($R_{load} = 15\ \Omega$ and $4.5\ \Omega$). Two horizontal lines correspond to the minimum input voltage $325 \cdot 0.9 = 292.5$ V and to the maximum input voltage $325 \cdot 1.1 = 357.5$ V. The two vertical lines give the frequency control region.

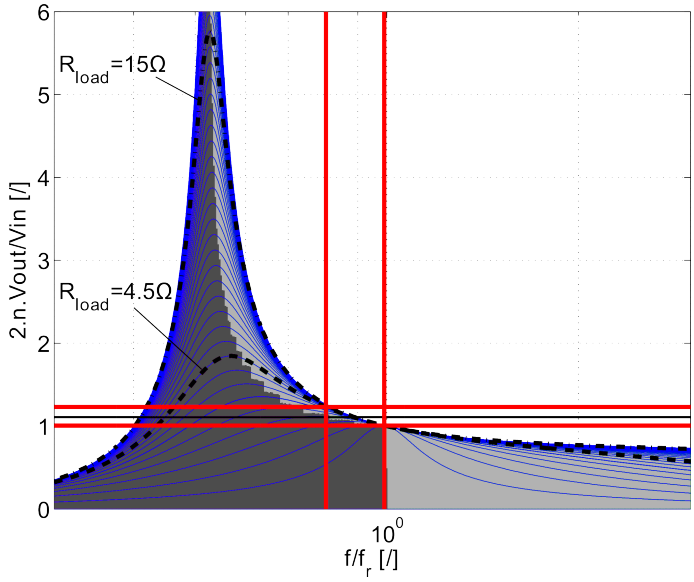


Figure 3.25: Amplification factor of the resonant tank of an LLC-converter; light grey = possible ZVS-region, dark grey = possible ZCS-region.

The possible ZVS-region is located to the left of the first resonance frequency $f_{r,1}$, above a specific curve, and is located to the right of the first resonance frequency.

The order of the resonance frequencies offers a specific advantage as compared to the LCC-converter. The first resonance frequency $f_{r,1}$ is greater than the

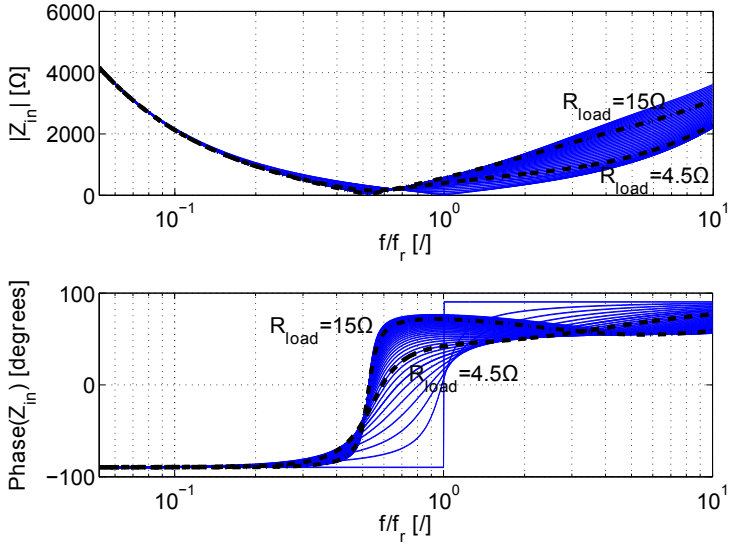


Figure 3.26: Amplitude and phase of the impedance, seen at the input of the resonant tank in an LLC-converter.

second, $f_{r,2}$, and the possible ZVS-region is located around $f_{r,1}$. This means that the operating region of the converter can be optimized around $f_{r,1}$.

There are two possibilities: in a first case, one takes the operating region to the right of $f_{r,1}$. In this case, the behaviour of the converter resembles that of a series-resonant converter.

In the second case, the operating region is taken to the left of $f_{r,1}$. ZVS can occur for loads not exceeding a specific maximum load. In this region, the converter combines the advantages of a parallel-resonant converter with those of a series converter. The higher the load, the more the LLC-converter resembles a series converter. However, when a short-circuit occurs at the load, the converter will operate in the capacitive region and a control algorithm should increase the switching frequency as fast as possible to a value higher than $f_{r,1}$ in order to have ZVS.

There are a couple of advantages when the converter operates to the left of $f_{r,1}$:

- The frequency control area is much smaller than when the converter is operated with switching frequencies greater than $f_{r,1}$ [Hsie 07][Chak 02].
- For a good choice of the components in the resonant tank, the behaviour of the converter resembles that of a parallel-resonant converter. This means that the effect of the output capacitance of the MOSFETs will

remain limited, as was discussed in the Sections about the series- and parallel-resonant converters.

However, an operation to the right of $f_{r,1}$ also has benefits. In that case, one can choose $f_{r,2}$ as low as one wants, meaning there is no upper limit for the value of L_{pr}. In the operation mode in the region to the left of $f_{r,1}$, the position of the second resonance peak, $f_{r,2}$ cannot be chosen in total freedom, because it determines the size of the frequency control interval. Therefore, for an operation in the region to the left of $f_{r,1}$, there is an upper limit for the size of L_{pr}.

One can also see from the amplification curves, that all the curves pass through the same point for a frequency equal to $f_{r,1}$. This is the load-independent point. Operating close to this point implicates that the frequency should vary only slightly when the load changes. Therefore, one strives to make the horizontal line of minimum amplification (at the greatest input voltage) pass through this load-independent point. In an LLC-converter, the region of ZVS lies around this point, but in an LCC-converter, the ZCS-region lies around it.

Finally, an added benefit of the LLC-converter with respect to an LCC-converter or a simple series- or parallel-resonant converter is that in an LLC-converter with transformer, the parasitic components of the transformer can be incorporated in the elements of the resonant tank. For L_{sr}, one can use the primary leakage inductance of the transformer and for L_{pr} the magnetizing inductance can be taken. For C_r, one has to use an external capacitance, providing a high-pass filtering effect so that the transformer will not saturate.

Therefore, an LLC-converter is preferred over an LCC-topology.

3.2.5 Series-parallel-resonant converters, type LLCC

A series-parallel-resonant converter of the LLCC-type is depicted in Fig. 3.27.

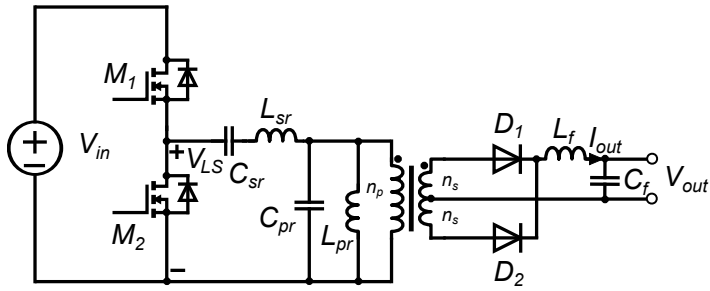


Figure 3.27: Series-parallel-resonant converter, type LLCC.

In this type of tank, three resonance frequencies are present:

$$f_{r,1} = \frac{1}{2\pi\sqrt{C_{sr}L_{sr}}} = f_r \tag{3.38}$$

$$f_{r,2} = \frac{1}{2\pi\sqrt{C_{sr}(L_{sr}+L_{pr})}} \tag{3.39}$$

$$f_{r,3} = \frac{1}{2\pi\sqrt{L_{sr}\frac{C_{sr}C_{pr}}{C_{pr}+C_{sr}}}} \tag{3.40}$$

with $f_{r,2} < f_{r,1}$ and $f_{r,3} > f_{r,1}$. The behaviour of this tank can again be studied using an AC-analysis (Fig. 3.28). The derivation of the amplification factor M and the equivalent output resistance is analogous to the method used when discussing the parallel-resonant converter, because the LLCC-converter also has an inductor in the output filter [Ang 02]:

$$R_{AC}^{prim} = \frac{\pi^2 n^2}{8} R_{load} \qquad M = \frac{n\pi^2 V_{out}}{4V_{in}} \tag{3.41}$$

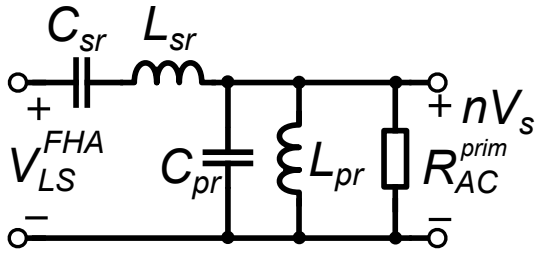


Figure 3.28: AC-equivalent circuit of the LLCC-converter

In Fig. 3.29, the amplification curve is shown in function of the frequency for an LLCC-converter with:

$C_{sr} = 350$ pF	$L_{sr} = 17$ μH
$C_{pr} = 100$ pF	$L_{pr} = 45$ μH
$V_{in} = 325$ V ± 10 %	$V_{out} = 15$ V
$n = n_p/n_s = 12$	$R_{load} = 4.5 - 15$ Ω

With the listed values of C_{sr} and L_{sr}, the first resonance frequency is $f_{r,1} = 1/(2\pi\sqrt{L_{sr}C_{sr}}) \approx 2$ MHz. From the phase characteristic (Fig. 3.30), it can be determined for which frequencies the tank is inductive and therefore where ZVS can be achieved. In Fig. 3.29, the inductive region, where ZVS can be achieved, is coloured light grey, and the capacitive region, where ZCS can occur,

is coloured dark grey. Notice that the border between the possible ZCS- and the ZVS-region is not located on the maxima of the amplification curves. Actually, the border between the two regions should be more smooth. The fact that it is not in the Figure, is due to a too coarse numerical interpolation. Also notice that the inductive nature of the resonant tank is a necessary condition for ZVS; however, the condition is not sufficient. Two magnification curves are plotted thicker: the curves of minimum and maximum load ($R_{load} = 15\ \Omega$ and $4.5\ \Omega$). Two horizontal lines correspond to the minimum input voltage of $325 \cdot 0.9 = 292.5$ V and to the maximum input voltage of $325 \cdot 1.1 = 357.5$ V. The two vertical lines give the frequency control region.

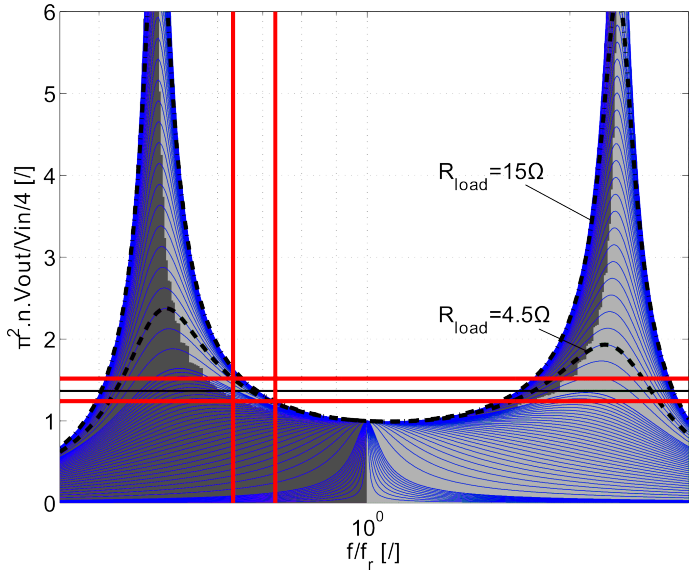


Figure 3.29: Amplification factor of the resonant tank of an LLCC-converter; light grey = possible ZVS-region, dark grey = possible ZCS-region.

As will be discussed in Section 3.5.9, a too large parallel resonant capacitance C_{pr} may cause loss of ZVS. This capacitance determines the position of the third resonance frequency $f_{r,3}$ and should remain small, otherwise ZVS is only attainable for frequencies higher than $f_{r,3}$, for all loads. Operation at these high frequencies would cause too much loss in the magnetic cores. For these reasons, an LLC-converter, and not an LLCC-converter, is constructed in this work to enable the power conversion demands of the project of this Chapter.

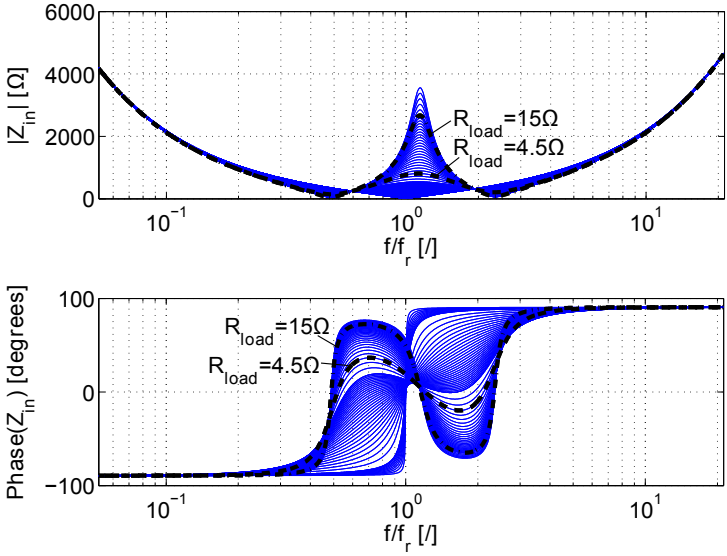


Figure 3.30: Amplitude and phase of the impedance, seen at the input of the resonant tank in an LLCC-converter.

3.3 Magnetic design

3.3.1 Losses in transformers

Because of the large input to output voltage ratio, a transformer will be used in the converter. This also offers advantages for safety because of the galvanic isolation such a device provides. The design of the transformer at multi-megahertz frequencies is to a great extent dependent on the losses. Losses in the magnetic material are called core losses and they can be subdivided in three categories:

1. *Hysteresis losses.* These losses are due to the irreversibility of the core material, characterized by its B-H-curve. The area of this curve is the energy which is lost every cycle and the power dissipation is therefore the product of this energy and the frequency:

$$P_H = f \oint H dB \tag{3.42}$$

In datasheets of core materials however, previous expression is written in a different form, based upon empirical data:

$$P_H = k_H f B_{max}^{\beta} \tag{3.43}$$

This expression is called a Steinmetz formula. β is equal to 2-3 for ferrites but is 1.5-2 for iron cores or for ferrites at high flux densities. B_{max} is the peak value of the flux density [Boss 05].

2. *Eddy current losses.* These losses are actually Joule losses, due to currents which are induced by a varying flux in the electrically conductive core material. They can be reduced by laminating the core, or by using powder cores, consisting of minuscule grains of magnetic iron, isolated from each other. Also these losses can be expressed with a Steinmetz formula [Boss 05]:

$$P_E = k_E f^2 B_{max}^2 \frac{1}{\rho} \tag{3.44}$$

This is also called Snelling's formula. ρ is the specific resistivity [Ω.m] of the core material. At higher frequencies, this expression should be adjusted: $P_E \propto f^n$ with $n > 2$, at constant flux density. Because ferrites are bad conductors, they have low eddy current losses and are ideally suited for high frequencies.

3. *Excess losses.* These are due to the interaction of the walls of the shrinking and expanding magnetic domains with the crystal lattice of the core material. A Steinmetz formula exists for the excess losses in magnetic iron or steel [Boss 05]:

$$P_{exc} = k_{exc}(f B_{max})^{3/2} \tag{3.45}$$

The magnetic domains can go into resonance with each other at high frequencies ($>$ 1 MHz) and the excess losses can therefore constitute a major part of the total core losses at these high frequencies [Good 02]. By using finely-grained materials, these losses can be decreased.

Apart from the core losses, there also exist *copper losses.* These are Joule losses in the copper windings. Copper has a specific resistivity, greater than zero, leading to Joule losses at zero frequency. At higher frequencies, Joule losses increase because eddy currents are induced in the windings, giving rise to the skin-effect or the proximity-effect. Litz-wire is used to mitigate the induction of eddy currents. It is composed of thin strands of copper conductors, being insulated from each other. The current density distribution is almost constant across the cross-section of the strands if the diameter of the strands is smaller than two times the skin-depth:

$$d_{Litz} < 2\delta = 2\sqrt{\frac{\rho}{\pi f \mu}} \tag{3.46}$$

with f the frequency, μ the permeability of the strand material and ρ its specific resistance.

3.3.2 Core materials for multi-megahertz transformers

In order to investigate what kinds of ferrite materials are useful for the application of this Chapter, the datahandbooks of different magnetics manufacturers were studied. The first manufacturer is Ferroxcube. According to the company, four kinds of materials are useful for coils and power transformers operating at high frequencies: 3F4 (up to 2 MHz according to the datahandbook), 3F45 (up to 2 MHz), 3F5 (up to 4 MHz) and 4F1 (up to 10 MHz). These are ferrites with a MnZn- and NiZn-composition. The second manufacturer is Magnetics. The materials that are withheld for the application of this Chapter are denoted by the letters R (up to 1.8 MHz according to the datahandbook), P (up to 1.8 MHz) and F (up to 1.5 MHz). The third manufacturer is Micrometals, offering the materials 2, 4, 6 and 7, for "radio-frequency" power electronics application. Finally, a last important manufacturer of core materials, is Epcos. This company offers the materials N27 (up to 100 kHz, according to its datahandbook), N87 (up to 500 kHz) and N49 and N59 (both up to 1 MHz). The material characteristics of all these materials are listed in Table 3.3. The most important characteristics are the relative permeability μ_r [1], the saturation flux density B_{sat}, the loss density P_V and the Curie temperature T_C, the temperature for which the core loses its magnetic properties and becomes demagnetized. When a cell is empty in the table or NA is inscribed, it means that there is no information about it available in the datahandbook.

From the Table, it is clear that the R-material from Magnetics and the 3F45 and 4F1 materials from Ferroxcube offer the lowest core losses at 3 MHz. The core loss densities of the materials of Epcos could not be evaluated at 3 MHz and where therefore left out of the consideration. However, the materials R, 4F1 and 3F45 are not easily available in many core-shapes. Therefore, we opt for the material 3F4, which is performing slightly less but which is however available in a greater variety of core shapes.

3.3.3 Selection of the core

The transformer specifications are given in Table 3.4. They are given for a load of 50 W and an apparent input power of 65 VA and for the highest switching frequency of 3 MHz.

Based on the data of this Table, the size of the core can be estimated making use of the total volt-ampère product of all the transformer windings [Boss 05]:

$$S_{tot} = \sum_{\text{all windings}} V_{rms} I_{rms} = \frac{325}{2} \cdot 0.4 + 15 \cdot 3.33 = 115 \text{ VA} \tag{3.47}$$

[1] The initial relative permeability is $\mu_{r,i} = \frac{1}{\mu_0} \lim_{\Delta H \to 0} \frac{\Delta B}{\Delta H}$
The amplitude relative permeability is $\mu_{r,a} = \frac{B}{\mu_0 H}$

Table 3.3: Commercial core materials for high-frequency power electronics applications.

Ferroxcube	$\mu_{r,i}$ [/]	B_{sat} [mT]	P_V [kW/m^3]	T_C [°C]	$\mu_{r,a}$ [/]
Conditions	25°C, 10kHz, 0.25mT	100°C, 10kHz, 1200A/m	100°C, 3MHz, 10mT		100°C, 25kHz, 200mT
3F4	900	350	220	200	1700
3F45	900	370	150	300	1700
3F5	650	340	900	300	1000
4F1	80	260	200	260	300
Magnetics	$\mu_{r,i}$ [/]	B_{sat} [mT]	P_V [kW/m^3]	T_C [°C]	$\mu_{r,a}$ [/]
Conditions	10kHz	1194A/m, 25^{o}C	3MHz, 10mT		
R	2300 ± 25 %	470	221	210	NA
P	2500 ± 25%	470	2469	210	NA
F	3000 ± 20%	470	222.5	210	NA
Micrometals	$\mu_{r,i}$ [/]	B_{sat} [mT]	P_V [kW/m^3]	T_C [°C]	$\mu_{r,a}$ [/]
Conditions			2.5MHz, 10mT		
MM 2	10	NA	700	NA	NA
MM 4	9	NA	NA	NA	NA
MM 6	8.5	NA	400	NA	NA
MM 7	9	NA	NA	NA	NA
Epcos	$\mu_{r,i}$ [/]	B_{sat} [mT]	P_V [kW/m^3]	T_C [°C]	$\mu_{r,a}$ [/]
Conditions	100°C	100°C, 10kHz, 1200A/m	100°C, 1MHz, 13mT		
N27	3200	410	200	220	NA
N87	4000	380	60	220	NA
N49	1702	370	20	240	NA
N59	850 (25°C)	370	NA	240	NA

In [Boss 05] it is shown that there is a relationship between the apparent power of a transformer and its size, when using natural convection of air as a means of cooling the transformer:

$$S_{tot} = A a_{ch}^{\gamma} \tag{3.48}$$

Here, A is a coefficient which is equal to $5 \cdot 10^6$ to $25 \cdot 10^6$ for ferrites at high frequency. γ is an exponent which is equal to $\gamma = 3.5 - 1/\beta$ with β the exponent of the peak flux density in the Steinmetz equation for the core losses. If β is 2, γ is 3. a_{ch} is a characteristic dimension of the core and is taken to be the

Table 3.4: Voltage, current and frequency specifications of the transformer of the LLC-converter.

$V_{in,rms}$	325/2 V ± 10 %
$I_{in,rms}$	0.4 A
V_{out}	15 V
I_{out}	3.33 A
f_s	3 MHz

largest dimension of the core. An EE20/10/5 core for example has an a_{ch} equal to 20 mm. For the project of this Chapter, a_{ch} is equal to:

$$a_{ch} = \left(\frac{S_{tot}}{A}\right)^{1/\gamma} = 0.017\ m \tag{3.49}$$

In the datahandbook of Ferroxcube, we then select all 3F4 cores having a largest dimension more or less equal to 17 mm. The number of primary windings is determined by:

$$N_1 = \frac{\psi_{pp}}{\phi_{pp}} \tag{3.50}$$

with ψ_{pp} the peak-to-peak flux linkage, or volt-seconds product, and ϕ_{pp} the peak-to-peak flux in the core:

$$\phi_{pp} = A_e B_{pp} \tag{3.51}$$

with A_e the effective area of the cross-section of the flux path and B_{pp} the peak-to-peak flux density in the core. The largest flux linkage is, for a duty cycle δ of 1/2, equal to:

$$\psi_{pp} = (V_{max}/2) \cdot \delta T_s = \frac{V_{max}}{4 f_s} \tag{3.52}$$

Once the number of primary windings is determined, the primary inductance can be calculated with the permeance A_L [H/turns^2], which is listed in the datasheet of the core:

$$L_1 = N_1^2 \cdot A_L \tag{3.53}$$

The number of secondary windings is:

$$N_2 = N_1/n \tag{3.54}$$

with n the transformation ratio, which is equal to $n = \lceil 325/2/15 \rceil = 11$.

The results of these calculations can be found in Appendix B. Two scenarios are modelled, each assuming that the transformer has an efficiency of 95%, and thus a loss total of $50 \cdot 0.05 = 2.5$ W. In a first scenario, the losses are

equally distributed over the core and copper windings: $P_{core} = 1.25$ W and $P_{cu} = 1.25$ W. In a second scenario, Litz-wire is used for the windings, drastically decreasing the copper losses: $P_{core} = 2$ W and $P_{cu} = 0.5$ W. There is also a third scenario, the worst case scenario: 2.5 W losses are core losses and there are also 1 W copper losses.

The core losses per unit volume are equal to $P_V = P_{core}/V_e$, with V_e the effective volume of the core, a quantity which is listed for each core in the Ferroxcube datahandbook. B_{pp} from equation (3.51) can be calculated as twice the peak value of the magnetic flux density B_{max}. To determine B_{max}, following Steinmetz expression exists [Ferr]:

$$P_V = C_m f^x B_{max}^y \cdot (ct_0 - ct_1 T + ct_2 T^2) \tag{3.55}$$

with P_V the core loss density in kW/m^3, T the temperature in °C, f the frequency in Hz, and for the 3F4-material $x = 2.8, y = 2.4, ct_0 = 0.67, ct_1 = 0.01 \cdot 10^{-2}, ct_2 = 0.34 \cdot 10^{-4}, C_m = 1.1 \cdot 10^{-11}$, for frequencies between 1 and 3 MHz. The calculations are performed at 3 MHz.

Next, the wire diameter is calculated, assuming that there are no eddy current losses in the copper windings. To do this, the copper losses P_{cu} are first distributed over the primary and secondary windings according to ([Boss 05], formula (2.16)):

$$P_{cu,1} = \alpha_1 P_{cu} \tag{3.56}$$

$$P_{cu,2} = \alpha_2 P_{cu} \tag{3.57}$$

with

$$\alpha_1 = \frac{N_1 I_{rms,1}}{N_1 I_{rms,1} + N_2 I_{rms,2}} \tag{3.58}$$

$$\alpha_2 = \frac{N_2 I_{rms,2}}{N_1 I_{rms,1} + N_2 I_{rms,2}} \tag{3.59}$$

The wire diameter is then calculated, assuming only DC Joule losses and no skin- or proximity-effect, according to (formula (2.19) of [Boss 05]):

$$d_i = \frac{2}{\sqrt{\pi}} I_{rms,i} \sqrt{\frac{\rho l_T N_i}{P_{cu,i}}}, \quad i = 1, 2 \tag{3.60}$$

with l_T the average length of one turn, a quantity which can also be found in the Ferroxcube datahandbook, and ρ the specific resistivity of copper ($\rho = 23 \cdot 10^{-9}$ Ω.m for annealed copper at 100°C).

Another quantity which is calculated, is the maximum allowed volumetric core loss density $P_{V,max}$. According to [Oren 04], if a temperature rise ΔT is allowed (for instance from 25 °C to 100 °C), the relationship between the total losses $P_{core} + P_{cu}$ (in mW) and the temperature rise is:

$$\Delta T = ((P_{core} + P_{cu})/A_{tot})^{0.833} \tag{3.61}$$

with A_{tot} the total surface area of the transformer in cm^2. From this expression, the maximum allowed core loss density (in kW/m^3) can be calculated.

Also the resonant capacitance C_r is calculated, for a first resonance peak at $f_0 = 1$ MHz:

$$f_0 = \frac{1}{2\pi\sqrt{L_1 C_r}} \tag{3.62}$$

For an allowed temperature rise of 75 K, all computed quantities can be found for the three scenarios in Appendix B, for different core types, all fabricated out of material 3F4, and having a maximum dimension of more or less 17 mm.

Some cells in the Tables of Appendix B are coloured. Dark grey cells denote that the volumetric core loss density exceeds the maximum allowed loss density. Thus, these cores should be excluded from further considerations. For the remaining cores of each type, the core with the largest C_r is selected, indicated by a light grey coloured cell. C_r is small at 3 MHz anyway, so from the remaining cores the core with the largest C_r is selected.

Three cores are suited for the application of this Chapter and they are listed in Table 3.5, for the worst case scenario. Actually the planar transformer has the lowest losses per unit volume and the largest resonant capacitance C_r, but it is more difficult to construct than a wound-type transformer, and therefore, for this project, the **RM8/I** core, made out of 3F4-material is selected. The

Table 3.5: Ferroxcube: three best core types.

Core name	Planar E PLT32/20/3/R	RM8/I	EFD20/10/7
P_{core} [W]	2.5	2.5	2.5
P_{cu} [W]	1	1	1
P_V [kW/m^3]	548.25	1024.59	1712.33
B_{max} [mT]	14.17	18.36	22.74
N_1	8	13	21
N_2	1	1	2
L_1 [μH]	10.24	16.9	27.78
C_r [nF]	2.47	1.50	0.91
d_1 [mm]	0.054	0.0382	0.0482
d_2 [mm]	0.22	0.16	0.20
$P_{V,max}$ [kW/m^3]	4068.52	2908.95	4273.89

maximum frequency we allow for this project is chosen to be **3 MHz**. In fact,

this is quite arbitrary, but the reasoning behind it is outlined here. Combining equations (3.50), (3.51), (3.52) and (3.55) yields a relationship between the loss density, the frequency and the number of windings:

$$P_V = C_m f^x \left(\frac{V_{max}}{8 f A_e N_1} \right)^y \cdot (ct_0 - ct_1 T + ct_2 T^2) \tag{3.63}$$

For a core temperature of $T = 100$ °C, and a maximum allowable core loss of 2.5 W, corresponding to a transformer efficiency of 95 % at 50 W output power, the maximum allowable frequencies for the RM8/I-core are listed in function of the number of primary windings in Table 3.6. Because it was expected that the number of primary windings will be around 13, the maximum frequency is set to be 3 MHz, when using the RM8/I-core.

Table 3.6: Selection of a maximum frequency for the RM8/I-core.

N_1	**allowable frequency [MHz]**	N_1	**allowable frequency [MHz]**
9	0.349	15	7.488
10	0.657	16	11.029
11	1.165	17	15.868
12	1.963	18	22.359
13	3.173	19	30.927
14	4.950	20	42.073

3.4 Design of the resonant tank of the converter

3.4.1 General design constraints

The converter needs to fulfill following design requirements:

- The switching frequency f_s should be greater than 2 MHz.
- The converter must supply a load between 15 and 50 W at 15 V. This means the maximum output current is

$$I_{out,max} = \frac{50 \text{ W}}{15 \text{ V}} = 3.33 \text{ A} \tag{3.64}$$

  And the corresponding load resistance is:

$$R_{load,min} = \frac{15^2}{50} = 4.5 \ \Omega \tag{3.65}$$

The minimum output current is

$$I_{out,min} = \frac{15 \text{ W}}{15 \text{ V}} = 1 \text{ A} \tag{3.66}$$

corresponding to a load resistance of

$$R_{load,max} = \frac{15^2}{15} = 15 \ \Omega \tag{3.67}$$

- The converter is designed for a maximum output power of 50 W. Assume that the efficiency is 90 %, then the input power is $P_{in} = 50/0.9 = 55.6$ W. At the minimum input voltage ($325 \cdot 0.9 = 292.5$ V), this gives the maximum input current:

$$I_{in,max} = \frac{55.6}{292.5} = 0.2 \text{ A} \tag{3.68}$$

- The maximum switching frequency is 3 MHz, as is discussed in the previous Section.

3.4.2 Using a more accurate model for the resonant tank; incorporating a transformer

To realize the LLC-tank, a transformer is used and the parasitic components of the transformer take the role of some of the resonant components of the LLC-tank. Referring to Fig. 3.23, the primary leakage inductance of the transformer $L_{lk,p}$ is used for the series resonant inductor L_{sr}. The magnetization inductance L_M of the transformer is used for the parallel resonant inductor L_{pr}. For the series capacitor C_r in the tank, an external capacitor is used. However, a transformer also has a secondary leakage inductance $L_{lk,s}$. Therefore, a more accurate AC-equivalent scheme is needed, which is depicted in Fig 3.31.

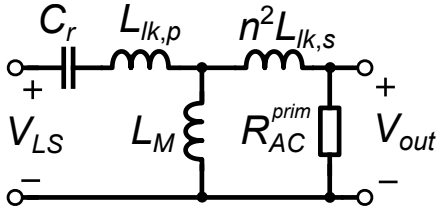


Figure 3.31: AC-equivalent scheme of the LLC-tank realized by a transformer and external capacitance C_r.

The equivalent load resistance, referred to the primary side of the transformer, has already been derived (cf. eq. (3.35)) and is:

$$R_{AC}^{prim} = \frac{8n^2}{\pi^2} R_{load} \tag{3.69}$$

It is however possible to retain the LLC-model without a secondary leakage inductance while at the same time taking this inductance mathematically into account (cf. Appendix C). To this end, one can define two equivalent resonant inductances [Fair 12]:

$$L_{sr}^{e} = L_{lk,p} + L_M//(n^2 L_{lk,s}) \tag{3.70}$$

$$L_{pr}^{e} = L_M + L_{lk,p} \tag{3.71}$$

The resonance frequencies of the resonant tank, with secondary leakage inductance, can be written in term of these equivalent inductances:

$$f_{r,1}^{e} = \frac{1}{2\pi\sqrt{C_r L_{sr}^{e}}} \tag{3.72}$$

$$f_{r,2}^{e} = \frac{1}{2\pi\sqrt{C_r L_{pr}^{e}}} \tag{3.73}$$

with $f_{r,2}^{e} < f_{r,1}^{e}$. $f_{r,2}^{e}$ is the same as $f_{r,2}$, the second resonant frequency in the simple LLC-tank without secondary leakage inductance. However, $f_{r,1}^{e}$ is smaller than $f_{r,1}$ [Fair 12].

3.4.3 Determining the optimal quantities in the resonant tank

In this work, an LLC-converter is designed. The upper working frequency is chosen to be equal to the maximum frequency, 3 MHz. For this reason, the highest resonance frequency, $f_{r,1}^{e}$, is chosen to be 3 MHz. This is a first condition restricting the size of the resonant components of the tank. A second condition can be imposed using the specification that the minimum working frequency should be greater than 2 MHz. We therefore demand that the lowest resonance frequency $f_{r,2}^{e}$ is around 2 MHz:

$$f_{r,1}^{e} = \frac{1}{2\pi\sqrt{C_r L_{sr}^{e}}} = 3 \text{ MHz} \tag{3.74}$$

$$f_{r,2}^{e} = \frac{1}{2\pi\sqrt{C_r L_{pr}^{e}}} \approx 2 \text{ MHz} \tag{3.75}$$

The last equation can also be written as:

$$f_{r,2}^{e} = \frac{1}{2\pi\sqrt{C_r L_{sr}^{e} \frac{L_{pr}^{e}}{L_{sr}^{e}}}} = \frac{1}{2\pi\sqrt{C_r L_{sr}^{e} m}} \tag{3.76}$$

with m the ratio:

$$m = \frac{L_{pr}^{e}}{L_{sr}^{e}} = 1 + \frac{L_M^2}{2L_M L_{lk,p} + L_{lk,p}^2} > 1 \tag{3.77}$$

In previous derivation of m, it is assumed that $L_{lk,p} = n^2 L_{lk,s}$. It is important not to take m too large or too small. If m is too small, the magnetic coupling between primary and secondary side is not adequate, because the magnetization inductance is too small and the leakage inductance too large. If m is too large, on the other hand, the leakage inductance is too small, thereby reducing the benefit of the amplification by having L^e_{sr}. For these reasons, one chooses $3 \leq m \leq 7$ ([Fair 12], p. 8).

A good design strategy places the minimal needed amplification at the highest resonance frequency $f^e_{r,1}$:

$$M_{min} = \frac{2n(V_{out} + V_{diode})}{V_{in,max}} = \sqrt{\frac{m}{m-1}} \quad \text{at } f = f^e_{r,1} \tag{3.78}$$

V_{diode} is the forward voltage drop across the diode of the output rectifier, and is approximately 0.7 V.

The optimal values of the resonant tank are determined with the following procedure: A first iteration is performed by letting the values of C_r, L_M, and $L_{lk,p}$ vary in following intervals:

- 100 pF $< C_r <$ 1000 pF in steps of 10 pF
- 1 μH $< L_M <$ 300 μH in steps of 1 μH
- 1 μH $< L_{lk,p} <$ 50 μH in steps of 1 μH

For every 3-tuple (C_r, L_M, $L_{lk,p}$), the highest resonance frequency $f^e_{r,1}$ and factor m are calculated and the 3-tuple is only withheld if the next two conditions are fulfilled:

- m should be between 3 and 7: $3 \leq m \leq 7$
- $f^e_{r,1}$ should be approximately 3 MHz:
  $3 \cdot 10^6[\text{Hz}] - 0.1\% \leq \frac{1}{2\pi\sqrt{C_r L^e_{sr}}} \leq 3 \cdot 10^6[\text{Hz}] + 0.1\%$

Only if the combination (C_r, L_M, $L_{lk,p}$) fulfills both the two previous conditions, the impedance and amplification characteristics of the tank are calculated. With these, the upper and lower working frequencies f_{max} and f_{min} are determined for a resistive load between 4.5 and 15 Ω. Then, a second filtering criterium is applied. Only if both

- $f_{min} > 2$ MHz, and
- $f_{max} < 3$ MHz

the combination (C_r, L_M, $L_{lk,p}$) is retained. Also the amplitude of the maximum current in the resonant tank is determined as:

$$I_{max} = \frac{4}{\pi} \frac{V_{in,max}}{2|Z_{min}|} \tag{3.79}$$

with $|Z_{min}|$ the minimum absolute value of the tank impedance at the highest load (4.5 Ω) in the frequency control interval $[f_{min}, f_{max}]$.

In order to select the most optimal configuration of the resonant tank, following issues should be taken into account:

- Best is to choose C_r the largest as possible, in order not to let the output capacitances of the MOSFETs of the half-bridge influence the behaviour of the tank too much. The output capacitances are typically of the order of 100 pF.
- The maximum current in the resonant tank should be as small as possible in order to minimize losses.
- The frequency control interval $\Delta f = f_{max} - f_{min}$ should be as large as possible, in order for the tank amplification not to be too sensitive to small frequency variations, and to assure an accurate operation.

The only parameter in previous search for optimal parameters for the resonant tank, which can still be varied, is the transformation ratio n. The calculations show that no valid solutions for (C_r, L_M, $L_{lk,p}$) can be found when $n < 13$. Therefore, we let n vary between 13 and 20. The results of the iteration analysis can be found in the Tables of Appendix D. From these Tables, some conclusions can be drawn:

- When C_r increases, the maximal current in the tank, I_{max} increases, for a constant transformation ratio n.
- For a constant C_r, I_{max} increases when the transformation ratio n increases.
- When n increases, the width of the frequency control interval Δf will decrease for a constant C_r.

Therefore, the most optimal tank is found with the smallest transformation ratio and smallest C_r, which is however at least substantially greater (for instance, a factor 5) than the output capacitances of the MOSFETs. We choose:

$n_{opt} = 13$	$C_{r,opt} = 0.49$ nF	$L_{M,opt} = 32$ μH	$L_{lk,p,opt} = 3$ μH

The optimization procedure to determine the optimal tank is a novel contribution of this work. The optimal permeance [H/turns^2] is then, assuming there are 13 turns in the primary winding and 1 turn in the secondary winding:

$$A_{L,opt} = \frac{L_1}{N_1^2} = \frac{L_{M,opt} + L_{lk,p,opt}}{N_{1,opt}} = \frac{32\mu\text{H} + 3\mu\text{H}}{13^2} = 207 \text{ nH/turns}^2 \quad (3.80)$$

3.4.4 Realization of the resonant tank

At 3 MHz, and a core temperature of 100 °C, the total core losses are calculated with eq. (3.63) in function of the number of turns in the primary winding (Fig. 3.32). It can be seen that for an optimal number of turns of 13, the core losses are about 2.5 W. The more turns, the lower the peak flux and the lower the core losses. In order to decrease the core losses even more and

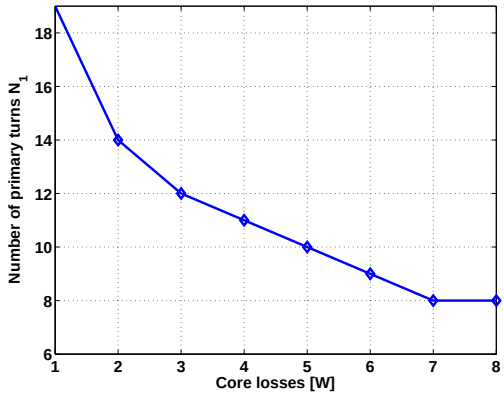


Figure 3.32: Number of turns in the primary winding of an RM8/I-3F4-core versus the core losses.

increase the efficiency of the converter, we opt to use more than 13 turns in the primary windings. We choose 17 turns, yielding core losses equal to 1.4 W. For a transformation ratio of 17, the selected parameters of the resonant tank are (cf. Table D.5):

$$\boxed{n = 17 \qquad C_r = 0.22 \text{ nF} \qquad L_M = 33 \ \mu\text{H} \qquad L_{lk,p} = 7 \ \mu\text{H}}$$

The cores, available in the RM8/I-3F4 gamma, are listed in Table 3.7. Therefore, we choose a core with a permeance of 100 nH/turns^2. Applying 17 turns, the realized primary inductance is:

$$L_1 = 17^2 \cdot 100 \cdot 10^{-9} = 28.9 \ \mu\text{H} \quad (3.81)$$

Table 3.7: Available permeances for an RM8/I-core of 3F4-material.

A_L [nH/turns^2]	$\mu_{r,eff}$	air gap [μm]	type number
$100 \pm 3\%$	49	1100	RM8/I-3F4-A100
$160 \pm 3\%$	78	610	RM8/I-3F4-A160
$250 \pm 3\%$	121	360	RM8/I-3F4-A250
$315 \pm 3\%$	153	270	RM8/I-3F4-A315
$400 \pm 3\%$	194	200	RM8/I-3F4-A400
$1700 \pm 3\%$	820	0	RM8/I-3F4

Litz-wire with 54 strands of AWG44 is used both for the primary winding and the secondary windings. AWG44 has a diameter of 0.05080 mm, smaller than twice the skin depth of copper at 3 MHz: $\delta = \sqrt{\rho/(\pi f \mu)} = 38$ μm. An advantage of using more turns than the optimal number, is that the core losses decrease. However, a higher transformation ratio also increases the current in the resonant tank. Table D.5 suggests a peak value of 1 A. Another disadvantage of increasing the transformation ratio is that the frequency control interval decreases in size: it becomes 284 kHz but this is still an acceptable value.

3.5 Equivalent model of the transformer

Because the resonant elements of the LLC-tank are part of the converter's transformer, it is important to accurately model the transformer. A high-frequency model for transformers is presented in [Lu 03]. A similar model, which shows only minor changes from that of [Lu 03], is shown in Fig. 3.33 and will be used for the transformer of this work. It takes the effects into account of inter- and intrawinding capacitances and also models the leakage flux, the copper and core losses and the finite magnetization inductance.

The transformer is made of a primary coil with 17 turns and two times a secondary coil of each a single turn (cf. Section 3.4.4). The top view of the winding scheme is shown in Fig. 3.34. A special winding technique, which is called a bank winding, is applied to minimize the voltage drops between two adjacent wires and hence the influence of the parasitic intrawinding capacitance (Fig. 3.35). The secondary coils have a common conductor as in Fig. 3.23. Two assumptions are made in order to simplify the model of Fig. 3.33:

1. It is assumed that both the secondary coils are identical. When the transformer is measured, the common conductor of the secondary coils is used and the measurements are done with the two coils in series. This technique is also advantageous for the accuracy of the results because measurements over two turns are more accurate than over one turn. The calculated quantities are then equally divided over the two secondary

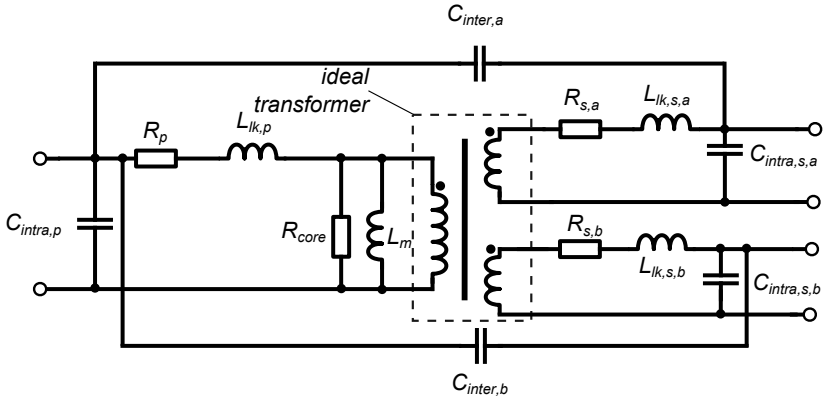


Figure 3.33: High-frequency transformer model.

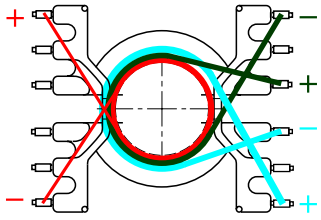


Figure 3.34: Top view of the transformer winding scheme.

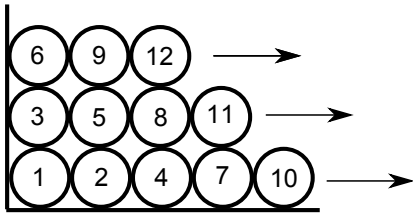


Figure 3.35: Bank winding for minimizing parasitic capacitances.

windings. This assumption implies that $R_{s,a} = R_{s,b} = R_s, L_{lk,s,a} = L_{lk,s,b} = L_{lk,s}, C_{inter,a} = C_{inter,b} = C_{inter}, C_{intra,s,a} = C_{intra,s,b}$.

2. A second assumption is that the intrawinding capacitances of the secondary sides can be neglected $C_{intra,s,a} = C_{intra,s,b} = 0$: . This is a valid assumption because the secondary coils have only one turn. This assumption allows a strong simplification of the transformer model. The transformer will be modelled as in Fig. 3.36.

A first estimate of the primary inductance can be made by multiplying the permeance A_L [H/turns^2] with the square of the number of turns. The permeance of the chosen RM8/I-core is 100 nH/turns^2 (cf. Section 3.4.4). This gives a primary inductance of:

$$L_1 = L_m + L_{lk,p} = N_1^2 \cdot A_L = 17^2 \cdot 100 \cdot 10^{-9} = 28.9\ \mu\text{H} \tag{3.82}$$

In order to determine the non-idealities of the transformer model, a couple of measurement experiments are carried out:

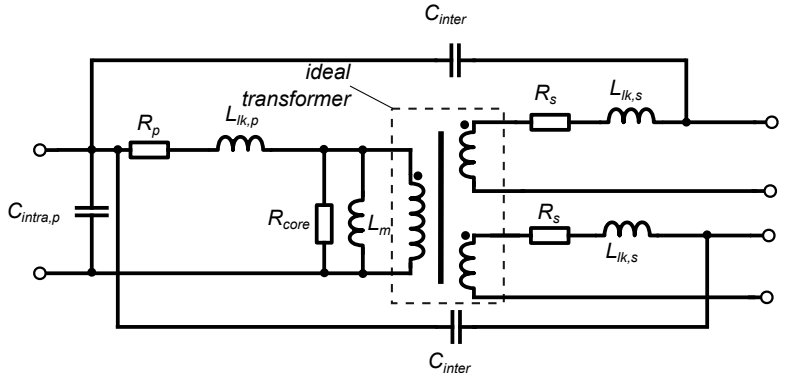


Figure 3.36: High-frequency transformer model, simplified with two assumptions.

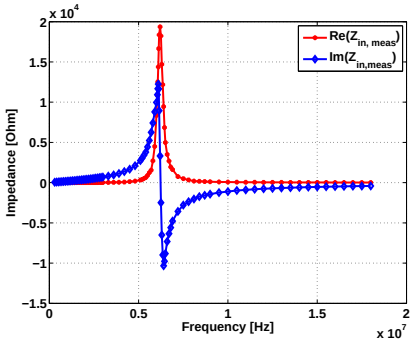
3.5.1 Measurement experiment 1: open-circuit test

In a first experiment, the secondary coils are kept open (i.e. not connected to a load), and the impedance of the transformer is measured from the primary side. The impedance can be measured with the volt-amp-meter method and a sine wave voltage can be applied at the primary side with a function generator. However, the function generators of the Electa laboratory can only reach frequencies of maximum 20 MHz, and as will be seen further on, higher frequencies are needed in the measurements. Therefore, the input impedance of the transformer, with secondary side open, is measured with a Hewlett-Packard 8753C Network Analyzer, having a frequency span between 300 kHz and 3 GHz. The results can be found in Appendix E, in Table E.1. The input impedance and its phase are shown in Figs. 3.37a-3.37b.

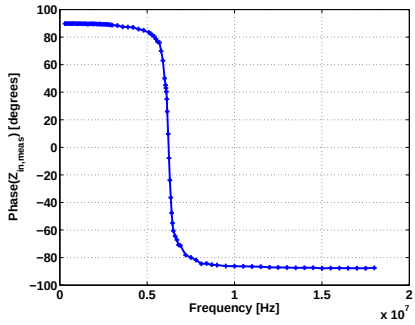
From the test, two conclusions can be drawn:

1. At low frequencies, the behaviour of the transformer is inductive, because the imaginary part of the input impedance and the phase of the input impedance are positive. In the open-circuit test, the transformer model is shown in Fig. 3.38. Between 2 and 3 MHz, the frequency range of interest of the project of this Chapter, the transformer in the open-circuit test is almost a perfect inductor, because the input impedance's phase is very close to 90°. The input inductance can be found by dividing the imaginary part of the input impedance by 2π times the frequency. If the primary coil's resistance and the core resistance[2] are neglected, the average value of the

[2]The core resistance models the core losses. In large power transformers, where the core is made from iron or magnetic steel, the core resistance is usually called the iron resistance. Because in this doctoral work ferrites are used for the core, it is chosen not to use the term 'iron resistance' but use 'core resistance' instead.



(a) Magnitude of the input impedance of the transformer, measured in the open-circuit test.



(b) Phase of the input impedance of the transformer, measured in the open-circuit test.

Figure 3.37: Input impedance of the transformer, measured in the open-circuit test.

input inductance between 2 and 3 MHz is $L_1 = L_m + L_{lk,p} = 33.67398$ μH, a value which corresponds well with the estimate of 28.9 μH.

2. From the resonance frequency, one can determine the value of $C_{intra,p}$. The resonance frequency is found where the imaginary part of the input impedance is zero: $f_{r,1} = 6.2407$ MHz. And because $f_{r,1} = 1/(2\pi\sqrt{L_1 C_{intra,p}})$, we find for the primary intrawinding capacitance:

$$C_{intra,p} = \frac{1}{(2\pi f_{r,1})^2 L_1} = 19.314 \text{ pF} \tag{3.83}$$

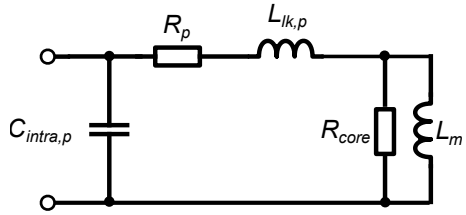
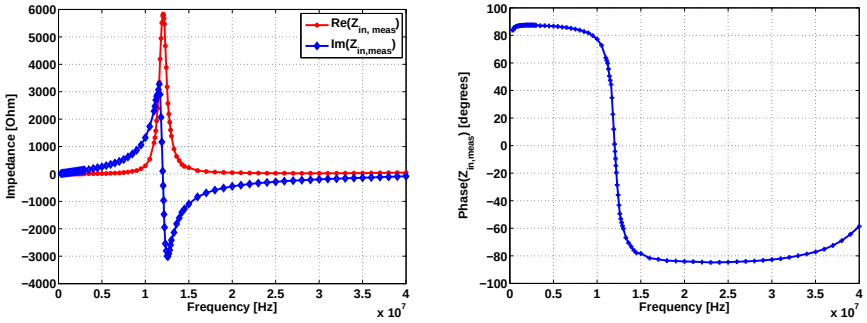


Figure 3.38: Transformer model during the open-circuit test.

3.5.2 Measurement experiment 2: short-circuit test

In a second experiment, the secondary coils are connected in series and short-circuited and the impedance of the transformer is measured from the primary side, with the Hewlett-Packard 8753C Network Analyzer. The results can be

found in Appendix E, in Table E.2. The input impedance and its phase are also shown in Figs. 3.39a-3.39b.



(a) Magnitude of the input impedance of the transformer, measured in the short-circuit test.

(b) Phase of the input impedance of the transformer, measured in the short-circuit test.

Figure 3.39: Input impedance of the transformer, measured in the short-circuit test

From the test, two conclusions can be drawn:

1. At low frequencies, the behaviour of the transformer is inductive, because the imaginary part and the phase of the input impedance are positive. In the short-circuit test, the transformer model, with the secondary elements referred to the primary side (as indicated by the primes), is shown in Fig. 3.40. Between 2 and 3 MHz, the frequency range of interest of the project of this Chapter, the input impedance is almost a perfect inductor in the short circuit test, because the phase is very close to 90°. The input inductance can be found by dividing the imaginary part of the input impedance by 2π times the frequency. Neglecting the coil resistances and the core resistance, the average value of the input inductance between 2 and 3 MHz is L_{eq}:

$$L_{eq} = L_{lk,p} + \frac{L_m(L'_{lk,s,a} + L'_{lk,s,b})}{L_m + L'_{lk,s,a} + L'_{lk,s,b}} = 7.353\ \mu\text{H} \tag{3.84}$$

2. From the resonance frequency, one can determine the value of $C_{intra,p} + C'_{inter}$. The resonance frequency is found where the imaginary part of the input impedance is zero: $f_{r,2} = 12.006$ MHz. And because $f_{r,2} = 1/(2\pi\sqrt{L_{eq}(C_{intra,p} + C'_{inter,a} + C'_{inter,b})})$, we find:

$$C_{intra,p}+C'_{inter,a}+C'_{inter,b} = \frac{1}{(2\pi f_{r,2})^2 L_{eq}} \Rightarrow C'_{inter,a}+C'_{inter,b} = 4.585\ \text{pF} \tag{3.85}$$

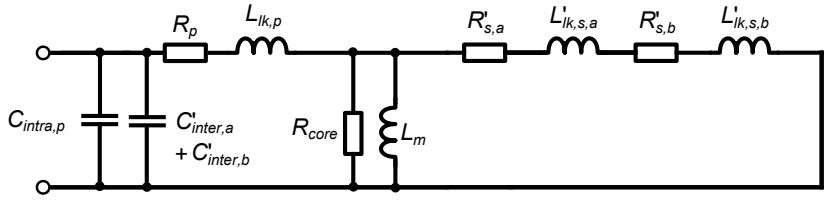


Figure 3.40: Transformer model during the short-circuit test.

3.5.3 Measurement experiment 3: frequency sweep with primary side open

In a third experiment, in order to find a relationship between the leakage inductances and the magnetization inductance, the secondary side of the transformer is fed with a sinusoidal voltage, supplied by a Rigol arbitrary waveform generator and the voltage on the primary side is measured. The measurements are done with a 500 MHz Tektronix TDS5054 Scope and a 500 MHz P6250 differential voltage probe. The results are shown in Table 3.8. The secondary voltage V_{sec} is referred to the primary side by multiplying it with the winding ratio $N_1/N_2 = 8.5$. This voltage is denoted by V'_{sec}. Then, the ratio of V_{prim} and V'_{sec} is determined. The average of this ratio between 2 and 3 MHz is $V_{prim}/V'_{sec} = 0.8964$. Neglecting the capacitances and the resistances, the voltage ratio is equal to:

$$\frac{V_{prim}}{V'_{sec}} = \frac{L_m}{L_m + L'_{lk,s,a} + L'_{lk,s,b}} \tag{3.86}$$

Table 3.8: Results of measurement experiment 3.

frequency [Hz]	V_{sec} [V]	V_{prim} [V]	ratio V_{prim}/V'_{sec}
500000	0.0768	0.493	0.7552
700000	0.1095	0.7055	0.7580
900000	0.145	0.936	0.7594
1100000	0.184	1.2	0.7673
1300000	0.226	1.495	0.7782
1500000	0.276	1.863	0.79418
1700000	0.34	2.3	0.7958
1900000	0.41	2.85	0.8178
2100000	0.508	3.65	0.8453
2300000	0.64	4.695	0.8631
2500000	0.832	6.36	0.8993
2700000	1.14	8.87	0.9154
2900000	1.57	12.8	0.9592

3.5.4 Measurement experiment 4: resistance measurement

Because Litz-wire is used with a sufficiently small strand diameter (cf. Section 3.4.4), it is assumed that the AC-resistance is not so much different from the DC-resistance. The resistance is determined with the volt-amp-meter method, where the voltage is measured with a Keithly 2000 multimeter and the current is measured with a resistive shunt (0.515 Ω for the primary shunt and 0.502 Ω for the secondary shunt; the resistances are determined with a Keithly 2000 multimeter). The voltage across the shunt is measured with a Fluke 309 multimeter. The measurement results are given in Table 3.9. The average of the measured resistance value is taken as the value of R_p or $R_{s,a} + R_{s,b}$:

$$R_p = 0.0634\ \Omega \quad \text{and} \quad R_{s,a} + R_{s,b} = 0.0271\ \Omega \tag{3.87}$$

Table 3.9: Results of measurement experiment 4.

V_{prim} [V]	I_{prim} [A]	R_p [Ω]	V_{sec} [V]	I_{sec}[A]	R_s [Ω]
0.07584	1.198	0.0633	0.0323	1.21514	0.0270
0.05553	0.876	0.0634	0.0210	0.7749	0.0270
0.04345	0.685	0.0634	0.0174	0.64343	0.0270
0.02712	0.427	0.0635	0.0126	0.46414	0.0271
0.0164	0.258	0.0635	0.0087	0.32271	0.0271

3.5.5 Determination of the magnetization inductance and the leakage inductances

Three equations are necessary, because there are three unknowns: $L_m, L_{lk,p}, L'_{lk,s,a} = L'_{lk,s,b}$. The equations were already stated in the previous Sections and are:

$$L_{lk,p} + L_m = L_1 = 33.674\ \mu\text{H} \tag{3.88}$$

$$L_{lk,p} + \frac{L_m(L'_{lk,s,a} + L'_{lk,s,b})}{L_m + L'_{lk,s,a} + L'_{lk,s,b}} = L_{eq} = 7.353\ \mu\text{H} \tag{3.89}$$

$$\frac{L_m}{L_m + L'_{lk,s,a} + L'_{lk,s,b}} = \frac{V_{prim}}{V'_{sec}} = 0.896 \tag{3.90}$$

Solving this set of equations, we find $L_m = 29.362\ \mu$H, $L_{lk,p} = 4.312\ \mu$H, $L'_{lk,s,a} = L'_{lk,s,b} = 1.696\ \mu$H.

3.5.6 Determination of the core resistance

Using the model of Fig 3.38 for the open-circuit test, the real part of the input impedance of the open-circuit test (Table E.1) is known. Because the values of

the magnetization inductance L_m, the primary leakage inductance $L_{lk,p}$, the primary resistance R_p and the primary intrawinding capacitance $C_{intra,p}$ have been calculated or measured in previous Sections, the core resistance R_{core} can be numerically calculated for each frequency. The results are shown in Fig. 3.41, and it can be seen that the core resistance is dependent on the frequency. For frequencies larger than 2 MHz and smaller than 3 MHz, the core resistance is more or less 40 kΩ. Taking this as an initial estimate, the value is subsequently adjusted in a PSpice-simulation until the input impedance of the transformer in the simulation agrees with the measured impedance. The final value for the core resistance is $R_{core} = 14850\ \Omega$.

3.5.7 Modelling the frequency-dependent resistance of the secondary windings

Simulating the short-circuit test in PSpice, using a value of 0.027/2 Ω for $R_{s,a}$ and $R_{s,b}$, does not give good results. The simulated resonance peak of the input resistance is much higher than the measured value, and for higher frequencies, there is a huge mismatch between the measured and the simulated input resistance. Adjusting R_p and R_{core} does not have a significant impact. Adjusting $R_{s,a} = R_{s,b}$ does. However, the discrepancy between simulation and measurement is still high, indicating that the problem is due to an inaccurate model for the frequency dependence of $R_{s,a} = R_{s,b}$.

In order to determine the model of the frequency dependence, the resistance of a piece of about 30 cm long of the wire of which the secondary coils are made, is measured with the Hewlett-Packard 8753C network analyzer between 300 kHz and 25 MHz. The measurement results are given in Table E.3 of Appendix E. In the second column, the real part of the input impedance is given. The third

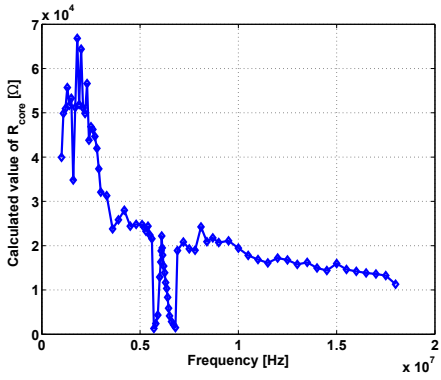


Figure 3.41: Calculated value of the core resistance.

column contains the resistance of the connector. The last column, which is the difference of the previous two, finally lists the resistance of the Litz-wire itself.

The theoretical formula for the resistance of Litz-wire can be found in [Term 43], page 37 of chapter 2, formula (8.a):

$$\frac{R_{ac}}{R_{dc}} = H + k\left(\frac{nd_s}{d_0}\right)^2 G \tag{3.91}$$

with: H the resistance ratio (AC to DC) of an individual strand when isolated (H is listed in a table in [Term 43]), G a constant, taking into account the proximity of neighbouring wires (G is listed in a table of [Term 43]), n the number of strands in the Litz-wire, d_s the diameter of an individual strand, d_0 the diameter of the wire and k a constant, dependent on n (k is listed in a table in [Term 43]). The wire in the transformer is AWG44-wire and employs 54 strands. Then, $n = 54$, $d_s = 0.0508$ mm and $d_0 = 0.68$ mm. The theoretical resistance is compared with the measurement results (Fig. 3.42). Also a second order polynomial fitting of the measurements is shown and a good agreement of the three curves is observed.

The resistance of the secondaries, which has a DC-value of $R_{s,a} = R_{s,b} = 0.0271/2\ \Omega$, is referred to the primary side and the DC-resistance is $R'_{s,a} = R'_{s,b} = 0.0271/2 \cdot 17^2 = 3.913\ \Omega$.

The second-order fit has an expression:

$$\begin{aligned} R_{ac} &= 2.9447 \cdot 10^{-16} f^2 + 2.7727 \cdot 10^{-8} f + 0.072579\ \Omega \\ &= 0.0702579 \cdot (1.0277 \cdot 10^{-16}\omega^2 + 6.0802 \cdot 10^{-8}\omega + 1)\ \Omega \end{aligned} \tag{3.92}$$

Therefore, the AC-resistance of an AWG44 wire with 54 strands, such as the transformer wire, is in general modelled as:

$$R_{ac,AWG44,\ 54\ strands} = R_{dc}(4.0573 \cdot 10^{-15} f^2 + 3.82029 \cdot 10^{-7} f + 1) \tag{3.93}$$

with f the frequency in Hertz, and R_{dc} the DC resistance of the wire. In PSpice, there exists a GLAPLACE element, which models a frequency-dependent conductance. An expression in the Laplace domain is needed as its argument. Thus, the expression of the GLAPLACE elements, modelling the conductances of the two secondaries, is, with $s = j\omega = j2\pi f$:

```
1/(3.913*(1+6.0802E-8*ABS(s)-1.0277E-16*s*s))
```
(3.94)

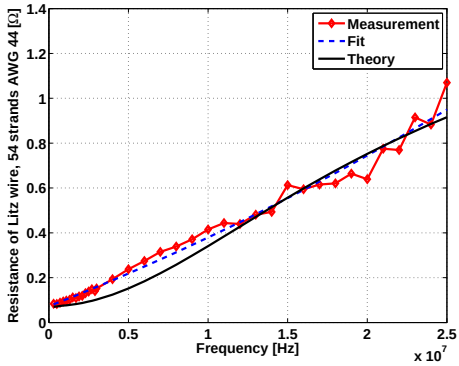


Figure 3.42: Frequency-behaviour of the resistance of a Litz-wire.

3.5.8 Final transformer model

The final, complete transformer model, referred to the primary side, for the transformer in the LLC-converter is shown in Fig. 3.43. It makes use of all the data of previous Sections. The expression for the frequency-dependent secondary coil conductances, implemented as GLAPLACE elements in PSpice, is given in eq. (3.94).

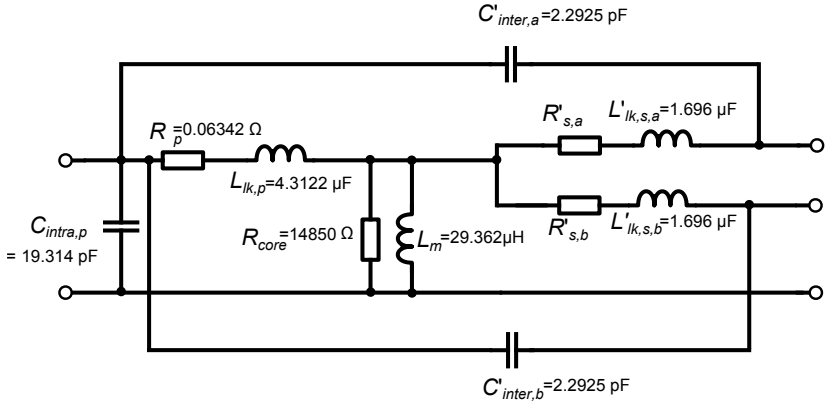
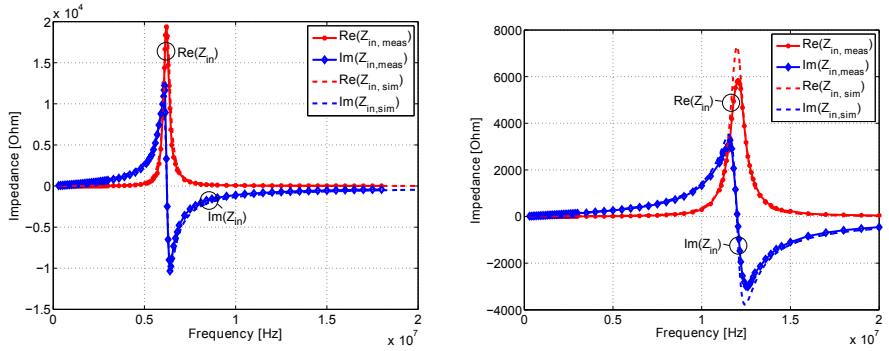


Figure 3.43: Final transformer model, referred to the primary side, of the transformer used in the LLC-converter.

With this model, the open-circuit and short-circuit tests are simulated in PSpice and simulation and measurement results are compared in Figs. 3.44a and 3.44b. There is a very good agreement between measurements and simulations, indicating that the lumped transformer model of Fig. 3.43 models reality well.



(a) Open secondaries.

(b) Short-circuited secondaries.

Figure 3.44: Comparison of measured and simulated input impedance of the transformer.

3.5.9 Amplification characteristic with the measured transformer parameters

The amplification characteristic is calculated, this time with the model of the transformer of Fig. 3.43. Only the (small) interwinding capacitances are neglected, because they make it hard to develop an analytic formula for the amplification factor M. However, their influence is small, and neglecting them only introduces a minor error. The characteristic is shown in Fig. 3.45, for a series resonant capacitor C_{sr} of 220 pF. The dashed line is the amplification curve for maximum load power, $R_{load} = 4.5\ \Omega$ and the dashed-dotted line is the curve for $R_{load} = 15\ \Omega$. The horizontal lines indicate the needed amplification for maximum and minimum input voltage. The two light grey vertical lines give the boundaries of the frequency control interval, and the thicker dark grey vertical line corresponds to a frequency of 2 MHz. The black solid curve is the boundary between the regions of ZCS (on the left-hand side) and ZVS (on the right-hand side). We therefore conclude that for the constructed transformer and for $C_{sr} = 220$ pF, ZVS is obtained and this occurs for frequencies greater than 2 MHz.

If the intrawinding capacitance were larger, however, the operating interval is spectacularly shifted to lower frequencies. This is shown in Figs. 3.46a-3.46c, for increasing intrawinding capacitances. Remember that the dark grey vertical line corresponds to 2 MHz. ZVS is in all these cases still obtained, though. Remark that in Fig. 3.46b the second light grey vertical line almost perfectly coincides with the dark grey vertical line.

However, when the intrawinding capacitance increases above 300 pF, ZVS can be lost, as is shown for $C_{intra,p} = 350$ pF in Fig. 3.47. Therefore, when designing

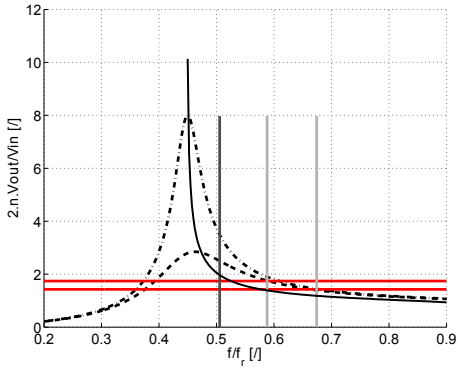
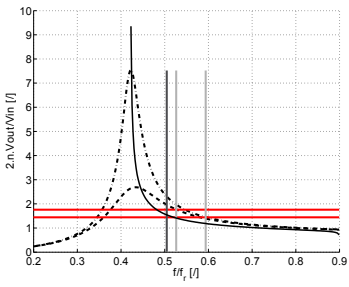
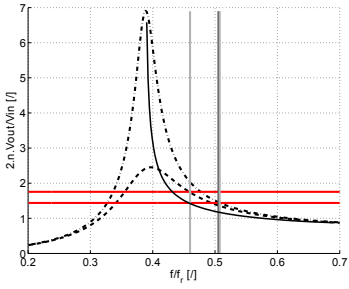


Figure 3.45: Amplification curve, calculated with the transformer model of Fig. 3.43, and with $C_{sr} = 220$ pF.

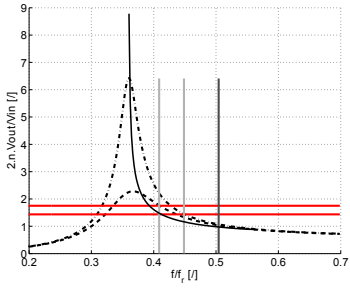
and building an LLC-converter, care must be taken so that the intrawinding capacitance remains small, for instance by employing a bank winding technique.



(a) $C_{intra,p} = 50$ pF.



(b) $C_{intra,p} = 100$ pF.



(c) $C_{intra,p} = 150$ pF.

Figure 3.46: Amplification curve for $C_{sr} = 220$ pF calculated with the transformer model of Fig. 3.43, except for the value of $C_{intra,p}$.

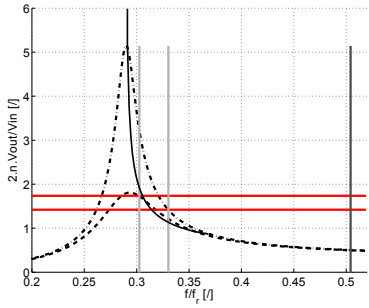
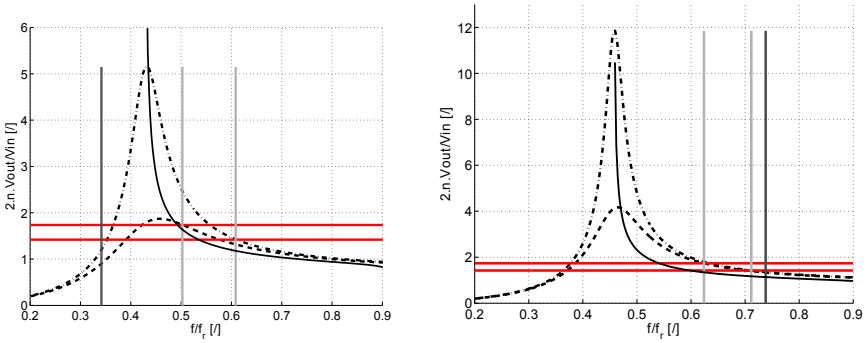


Figure 3.47: Amplification curve for $C_{sr} = 220$ pF calculated with the transformer model of Fig. 3.43, except $C_{intra,p} = 350$ pF.



(a) Amplification curve with the measured tank parameters and $C_{sr} = 100$ pF.

(b) Amplification curve with the measured tank parameters and $C_{sr} = 470$ pF.

Figure 3.48: Sensitivity of the amplification factor to the series resonant capacitance.

Let us continue the sensitivity analysis and investigate what happens when the series resonant capacitance C_{sr} changes. The effect is shown in Figs. 3.48a-3.48b. The dark grey vertical line again corresponds to 2 MHz. It can be seen that the operating frequency interval shifts to lower frequency values, and even under 2 MHz for too large values of C_{sr}, but ZVS is in the Figures never lost. An analysis shows that even for values above 470 pF, ZVS is maintained.

3.5.10 PSpice model for an ideal transformer

The transformer model is shown in Fig. 3.43. All the elements are referred to the primary side. In order to use this model in PSpice, an ideal transformer must be placed after the circuit of Fig. 3.43. The ideal transformer can be modelled in

Spice by two inductors being coupled with each other with the K-element, and a coupling factor of 1, and it is also possible to use dependent voltage and current sources for the modelling [Mear, Herb 08, Sand 06]. The second approach is chosen here, because the first sometimes gives rise to convergence problems for a project like this, where because of the high switching frequency small reactive components are present, but where at the same time the coupled inductors of the ideal transformer have large inductance values. The model of the ideal transformer is shown in Fig. 3.49. As can be seen, a voltage controlled voltage source and a current controlled current source are used. Also, a zero volts DC-source V_V1 is present and the positive direction of the current I(V_V1) flowing through this source is indicated by an arrow. The Spice nodes are also depicted. In PSpice, the transformer ratio n is input as a parameter, using the PARAM-element. The Spice netlist of the subcircuit *IT* describing an ideal transformer is then as below:

```
.SUBCKT IT 1 2 3 4
V_V1 5 3 DC 0
F_F1 1 2 V_V1 {1/n}
E_E1 5 4 1 2 {1/n}
.ENDS
```

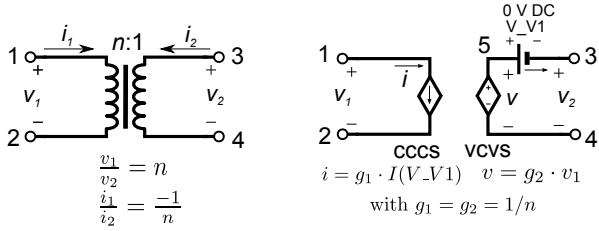


Figure 3.49: Modelling an ideal transformer with dependent sources in PSpice.

3.5.11 Investigation of the feasibility of an air-core transformer

Because inductances are often inversely proportional with the frequency, inductance values can become so low at high frequencies, that the needed permeability of the core may assume the value for air. An apparent advantage of air-cores is the absence of core losses. Let us therefore investigate if and when the use of an air-core is feasible. Reference [Lund 85] gives a formula for the inductance of a single-layer solenoid. a is the radius of the coil, b is its axial length. When a wire is used of diameter 1 mm, the inductance is plotted in function of a and b in Fig. 3.50. Contour lines are drawn for inductances of 1, 10, 20, 30, ..., 100 μH. Compare this with the primary inductance of the transformer of this Chapter, being $L_1 = 33.7$ μH. The crosses mark the points where the volume of the solenoid coil is minimal for a specific inductance value. The straight line is the set of points where the diameter of the coil is equal to its length. To have an inductance of 30 μH, the radius and axial length for a minimal volume are 0.18858 mm and 1.335 m, yielding a volume of 0.1492 cm^3. For a square cylindrical coil of 30 μH, the diameter and axial length are 2.11 cm,

yielding a volume of 7.34 cm^3. The outer dimensions of the RM8/I core set are 1.64 cm x 2.32 cm x 1.1 cm, yielding a volume of 4.18528 cm^3, which is of the same order as the volume of the square air-core cylindrical coil. It can be concluded that air-core inductors and transformers are feasible to use in the power converter of this Chapter. However, it can be expected that the magnetic coupling between primary and secondaries will be not good at all when using an air-core, and that the constraint on m of Section 3.4.3 cannot be fulfilled. Therefore, for transformers, ferrite cores are still preferred. However, for inductors, previous calculation shows that air-cores are small and because they are not subject to magnetic losses or saturation, their use can be very beneficial.

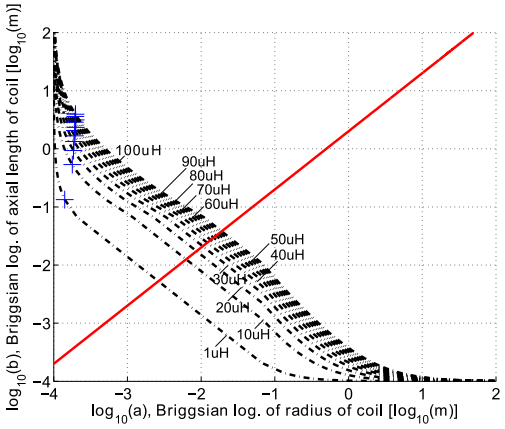


Figure 3.50: Inductance of a single-layer solenoid in function of its coil radius a and axial length b.

3.6 Design and realization of the converter

3.6.1 Choice of the MOSFETs

The minimum breakdown voltage of the MOSFETs should be larger than the maximum input DC voltage of the converter, $325 + 10\% = 357.5$ V. Also ringing can occur, due to parasitics in the components and the PCB-tracks, and therefore a safety factor should be used. We select for this reason only MOSFETs with a saturated drain-to-source breakdown voltage BV_{DSS} of 500 V or larger.

In the analysis of the resonant tank, a maximum resonant current of 1 A through the MOSFETs is observed. Also a safety factor is taken into account, and only MOSFETs capable of conducting a minimum DC current of 2 A are withheld.

The figure of merit (see Section 2.3.8) is the inverse of the product of on-resistance and gate charge. The first characterizes the conduction losses, the second the switching losses and the current the gate-driver should deliver to turn the MOSFET on and off. Both of these quantities, $R_{on,stat}$ and Q_g, are listed for some withheld MOSFETs in Table F of Appendix F. The on-resistance is less important at high frequencies. We therefore base our selection on the gate charge Q_g. Another contribution to the switching losses comes from the dissipation of the energy which is stored during the off-time in the output capacitance C_{oss}, in the channel resistance when the MOSFET switches on. A quantity which characterizes this contribution to the switching losses is C_{oss}, and it is also listed in the Table. It is however of much lesser importance when the turn-on occurs at zero voltage.

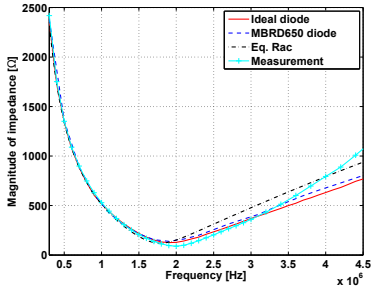
The best MOSFET, with the smallest Q_g, is the STD3NM50 component. This component was however not available at the supplier at the time when the project was carried out, as were other well-performing devices, and therefore the component FQP2N60 is selected.

3.6.2 Application of the zero voltage switching conditions of Section 3.1.3 to the case of the FQP2N60C MOSFET

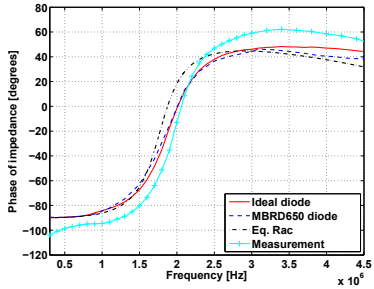
The conditions for zero voltage switching of Section 3.1.3 will now be applied to the case of the chosen MOSFET, FQP2N60C.

The input impedance of the resonant tank, followed by the output rectifier and resistive load, is measured for a load of 4.5 Ω and for a load of 15 Ω, with an arbitrary waveform generator. It supplies a high enough voltage and current in order to bring the output rectifier diodes into conduction. Alternatively, a calculation based on the transformer model of Fig. 3.43 and on the value of the equivalent AC-resistance (eq. (3.35)) could be performed to determine the input impedance, but it was deemed that a direct measurement of the input impedance would be more accurate. The measurement results of the input impedance of the resonant tank, followed by the output rectifier and a resistive load, are compared with simulations results in Fig. 3.51. The simulations are done with a sine input voltage with amplitude $4 \cdot 325/(2\pi)$ V, and in the output rectifier ideal diodes or the MBRD650CTG diodes are subsequently used, or, the output rectifier and load are replaced by the equivalent AC-resistance (eq. (3.35)). It can be seen that the small-signal measurements of the input impedance approximate the values given by the large-signal simulations well,

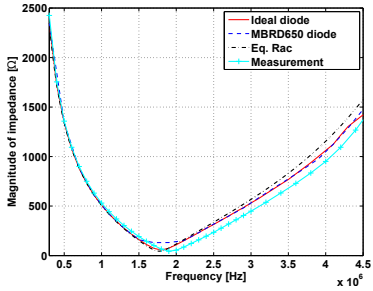
certainly in the range from 2 to 3 MHz, and can therefore be used to calculate the resonant current.



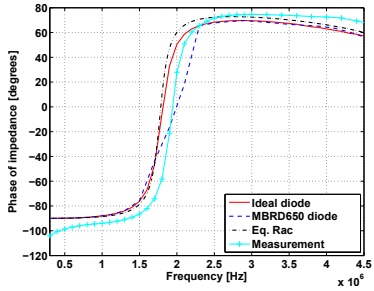
(a) Magnitude of the input impedance for a load resistance of 4.5 Ω.



(b) Angle of the input impedance for a load resistance of 4.5 Ω.



(c) Magnitude of the input impedance for a load resistance of 15 Ω.



(d) Angle of the input impedance for a load resistance of 15 Ω.

Figure 3.51: Input impedance for the resonant tank, output rectifier and load, for two different load conditions.

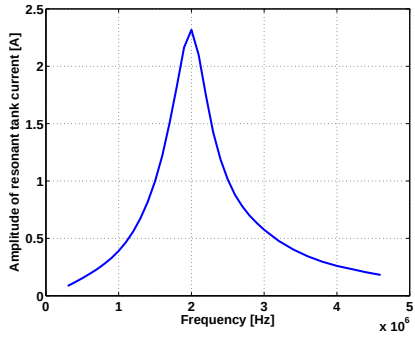
The first harmonic of the current flowing through the resonant tank is then calculated as follows:

$$I = \frac{4 \cdot 325/2}{\pi Z_{in}} \tag{3.95}$$

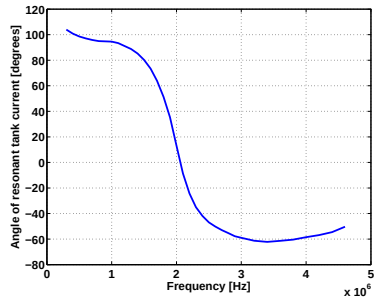
with Z_{in} the measured input impedance of the tank, rectifier and load network. I is a complex number, and its magnitude and phase are depicted for the two different load conditions in Figs. 3.52a-3.52d.

The datasheet of the FQP2N60C MOSFET shows the voltage dependence of its output capacitance C_{oss}. This curve is numerically integrated from 0 till 325 V and the result is $Q/2$, with Q the charge of the total output capacitance of the complete half-bridge, consisting of two MOSFETs, as explained in Section 3.1.3.

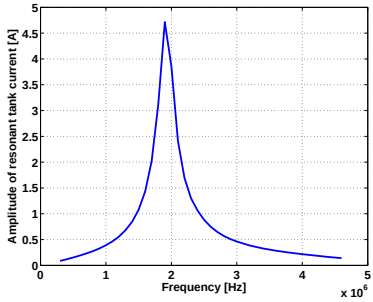
The lower and upper bound on the dead time in order to have zero voltage switching, are then given by eqs. (3.8) and (3.9). There is a lower bound because



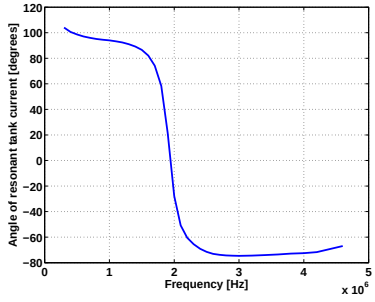
(a) Magnitude of the resonant tank current for a load resistance of 4.5 Ω.



(b) Angle of the resonant tank current for a load resistance of 4.5 Ω.



(c) Magnitude of the resonant tank current for a load resistance of 15 Ω.



(d) Angle of the resonant tank current for a load resistance of 15 Ω.

Figure 3.52: Resonant tank current for two different load conditions.

the current in the resonant tank must have sufficient time in order to completely discharge the output capacitance of the MOSFET that is about to switch on. There is also an upper limit on the dead time because when the dead time is too long, the resonant tank current changes its direction and starts to charge the output capacitance, after first having discharged it while its direction was opposite. The lower and upper bounds are shown in Fig. 3.53 and 3.54. When the lower bound is higher than the upper, no ZVS can be achieved. From the Figures, it can be seen that ZVS is for the converter of this work more easily achieved at lighter load than at higher load, even though at higher load, one would intuitively expect a higher resonant current to flow and one would expect that a shorter dead time is needed in order to discharge the output capacitance. The analysis of this Section shows that this reasoning is false. At light load, ZVS is achieved from 1.95 MHz till 3.577 MHz. At high load, ZVS is achieved from 2.17 MHz till 3.6 MHz, if the dead time is adequately chosen, as shown in the Figures. At 2.17 MHz, for a high load, the dead time should be 48.2 ns and at 3.6 MHz, it should be 94.7 ns. For frequencies in between, the dead

time has a lower bound and an upper, and the difference between the two is maximum 36 ns, at 2.5 MHz. This proves that for both load conditions, and for the designed resonant tank, the FQP2N60C MOSFET can achieve ZVS in a wide frequency region between 2 and 3 MHz.

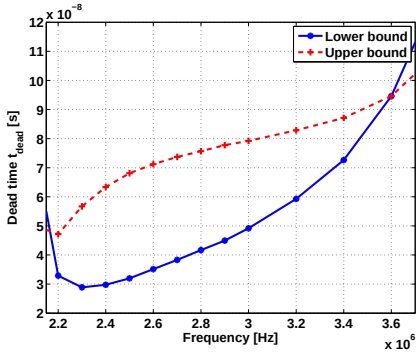


Figure 3.53: Bounds on the dead time for the FQP2N60C MOSFET and a load of 4.5 Ω.

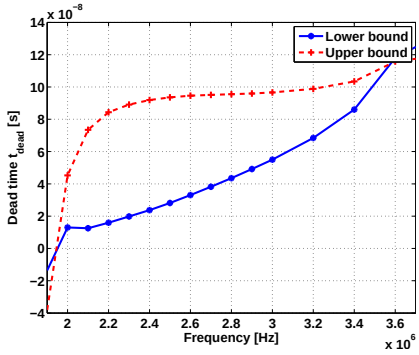


Figure 3.54: Bounds on the dead time for the FQP2N60C MOSFET and a load of 15 Ω.

3.6.3 Design and realization of the output rectifier

A half-wave rectifier can be used at the output of the transformer. This only requires a single diode, but the disadvantage is that the output voltage ripple will be double of the ripple in a rectifier which uses both lobes of the sine voltage wave. Therefore, with a half-wave rectifier, the output filter after the half-wave rectifier will be larger. For this reason, this topology is not used in this work. A full-wave rectifier will therefore be used. This is a rectifier, making use of both the positive and the negative lobe of the sine voltage wave. A so-called Graetz-bridge can be used, consisting of four diodes ([Horo 89], p. 44-47), but in this work, the full-wave rectifier is constructed with two diodes, and the transformer is given a centre tap (Fig. 3.55). Each diode in the Graetz-bridge has to be able to block the output voltage but in the design of Fig. 3.55, each diode has to be able to withstand twice the output voltage. Consider the time interval where the upper diode conducts. At point A the potential is $V_{out} + V_{diode}$ with respect to point C. V_{diode} is the forward diode drop. At point B, the potential will be $-(V_{out} + V_{diode})$, with respect to point C, because of the polarity of the secondary transformer windings. At point D, the potential is always, in steady-state, V_{out}. When the upper diode conducts, the lower one blocks a voltage which is equal to the potential at point D minus the potential at point B. This is equal to $V_{out} - (-(V_{out} + V_{diode})) = 2V_{out} + V_{diode}$. The forward diode drop therefore increases slightly the voltage a diode has to block.

We choose Schottky rectifiers for the diodes, because of their lower forward voltage drop than p-n-diodes [Bern], because the output voltage itself is quite low. Also the fact that they are unipolar devices is advantageous for this project. This makes them fast and the switching losses are low because the reverse recovery current is orders of magnitude smaller than in p-n-diodes [Bern]. The Schottky diode MBRD650CTG manufactured by ON Semiconductor is chosen for the converter's output rectifier, being able to conduct 6 A and block 50 V.

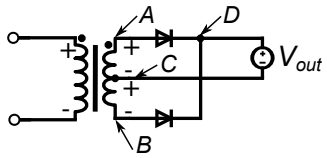


Figure 3.55: Output rectifier of the LLC-converter.

3.6.4 Design and realization of the output filter

For the output filter, a CLC-filter is chosen (Fig. 3.56). It is also called a π-filter. This type of filter has more degrees of freedom than a C- or LC-filter. Therefore, the same specifications can be reached with smaller filter components. The voltage across the input of the filter is a rectified sine, applied by the secondaries of the transformer. In the ideal case, this waveform only contains the fundamental component.

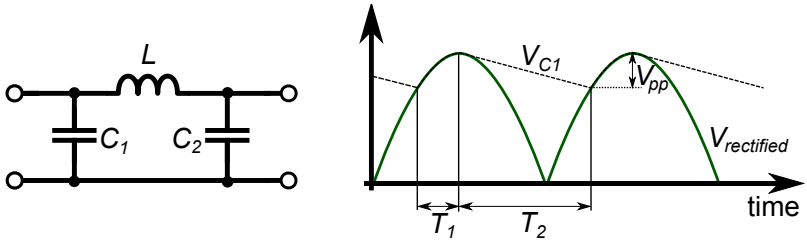


Figure 3.56: CLC-output filter of the LCL-converter: topology and waveforms.

In steady-state operation, two intervals can be distinguished (Fig. 3.56): in the first interval, the rectified voltage is bigger than the voltage across the capacitor C_1 of the filter. This means that this capacitor is being charged. When the rectified voltage reaches its maximum value, this interval ends and a second starts. In the second interval, the rectified voltage decreases and the capacitor discharges slowly. The discharge time is proportional to the capacitance value.

In the first interval, with a duration of T_1, the capacitor C_1 is charged with a charge $V_{pp}C_1$. In the second interval, with duration T_2, this charge is lost, and

is equal to $I_{pp}T_2$. When T_2 is much bigger than T_1, $T_2 \approx T/2 = 1/(2f)$, with f the frequency and T the period of the sine wave, offered by the transformer, before it is being rectified. Equating $V_{pp}C_1$ with $I_{pp}T_2$ then leads to:

$$C_1 = \frac{I_{pp}}{2fV_{pp}} \tag{3.96}$$

For the maximum load of the converter, the following specifications hold:

- $V_{pp} = 100$ mV
- $I_{pp} = \frac{V_{pp}}{R_{load,min}} = \frac{100 \text{ mV}}{4.5 \ \Omega} = 22.2$ mA
- $f_{min} = 2$ MHz

leading to a capacitance value of $C_1 = 56$ nF.

The inductor L can be calculated as follows. The voltage across the inductor and the current through it, are related by:

$$V = L\frac{di}{dt} \tag{3.97}$$

In this equation, only the AC-components of the voltage and current are important because when $i = I_{dc} + i_{ac}$, then $di/dt = di_{ac}/dt$. In previous equation, V can be replaced by V_{pp}, di by I_{pp}, and dt by $T_2 \approx T/2 = 1/(2f)$. We thus have:

$$L = \frac{V_{pp}}{2fI_{pp}} = 1.125 \ \mu\text{H} \tag{3.98}$$

To determine the second capacitance value, C_2, we make use of the expression for the ripple factor γ [Kish 05]. This factor is defined as:

$$\gamma = \frac{V_{\text{AC}-\text{component},rms}}{V_{dc}} \tag{3.99}$$

with $V_{\text{AC}-\text{component},rms}$ the RMS-value of the AC-component of the ripple voltage and V_{dc} the DC-value of the output voltage. For a triangular voltage ripple, the RMS-value is equal to:

$$V_{AC-component,rms} = \frac{V_{pp}}{2\sqrt{3}} \tag{3.100}$$

The ripple factor is given by [Kish 05] on page 166:

$$\gamma = \sqrt{2}\frac{X_{C1}}{R_{load}}\frac{X_{C2}}{X_L} = \frac{\sqrt{2}}{R_{load}}\frac{1}{\omega^3 C_1 C_2 L} \tag{3.101}$$

For a maximum load, a frequency of 2 MHz and a peak-to-peak voltage ripple of 100 mV, C_2 is then 1.3062 μF. In practice, higher harmonics will be present

in the output waveform of the rectifier. Also, previous calculation of the values of C_1, L and C_2 is based on the simplifying assumption that the peak-to-peak voltage across each of the three elements is the same and is equal to V_{pp}. For these reasons, we choose bigger values for the components C_1, C_2 and L:

- $C_1 = 220$ nF. We choose the 50 V MCCA000479c ceramic capacitor from Multicomp, which has a 1206 size.
- $L = 15$ μH. We choose the ferrite SRR1260-150M inductor by Bourns, allowing 4.6 A and having a self-resonance frequency of 17.6 MHz.
- $C_2 = 10$ μF. We choose the 50 V C4532Y5V1H106Z ceramic capacitor from TDK, having a 1812 size.

3.7 Design and realization of the half-bridge gate-driver

In Section 2.2.3, a fast gate-driver for a single transistor is developed. However, the project of this Chapter includes a half-bridge, consisting of two MOSFETs. They should be turned on and off alternately, and there should be a dead-time between the interval that the high-side transistor of the bridge is on and the interval that the low-side transistor is on, to avoid short circuits. For multi-megahertz converters, the efficiency of the total converter system is impacted by the dissipation in the gate-driver as well, and therefore, resonant gate-drivers are often employed, where the gate resistance is replaced with a resonant non-dissipative network. In this work however, a hard-switching gate-driver is designed, switching between 0 and 12 V and having a user-adjustable dead-time. A simplified diagram of the design is shown in Fig. 3.57 and the full schematic and bill of materials (BOM) can be found in Appendix G.

Two XOR-gates are used and are fed with a signal a by a pulse source, generating, with a little delay, the signal a itself and its complementary, $\overline{a}$. This is true because for XOR-gates, the truth table is:

Table 3.10: Truth table of an XOR-gate.

input 1	input 2	output
0	0	0
0	1	1
1	0	1
1	1	0

The signals a and $\overline{a}$ are applied to an RCD-network. The resistor R and capacitor C make the rising edges of x and y rise more slowly, in an exponential

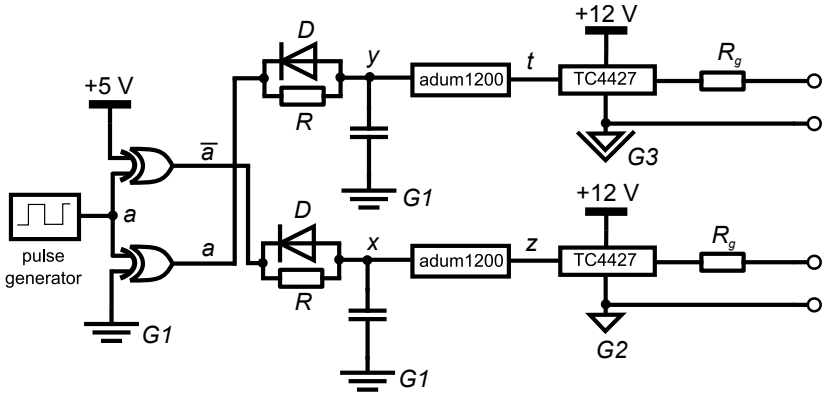


Figure 3.57: Simplified schematic of the half-bridge gate-driver.

fashion with a time constant RC. The diode D, however, allows the falling edges of x and y to fall down almost without a delay. This is explained in Fig. 3.58.

The Adμm1200 is a high speed digital isolator, providing a galvanic insulation between input and output, but apart from that and also a delay, it just provides the identity operation on its input. It has a Schmitt-trigger with a hysteresis function at its input. If the lower hysteresis level is $H-$ and the upper is $H+$, Fig. 3.58 clarifies how the circuit of Fig. 3.57 provides a dead-time. The capacitor C is 100 pF and the resistor is a potentiometer: a resistance value of around 100 Ω provides a dead-time of about 10 ns. Because of the digital isolator, the grounds $G1$, $G2$ and $G3$ are different. Finally, the gate-driver chip which is used, is the TC4427 chip from Microchip.

The reason why the driver chip TC4427, providing 3 A if the two channels are placed in parallel, is chosen over the TC4422, which provides 9 A, is that the TC4427 is more suited to operate at higher frequencies. This will now be explained. There are 3 kinds of losses in a hard-switched gate-driver:

1. The losses in the gate resistor, P_R. These losses are equal to the switching frequency, multiplied by the energy stored in the gate capacitor of the MOSFET that is driven:

$$P_R = f_s Q_g V_{DD} \tag{3.102}$$

with f_s the switching frequency, Q_g the gate charge of the MOSFET that is driven and V_{DD} the voltage level to which the gate is raised. For the gate-driver of this Chapter, $V_{DD} = 12$ V, f_s is maximum 3 MHz, and Q_g of the FQP2N60 MOSFET is equal to about $Q_g = 9$ nC at 325 V. This gives a loss of $P_R = 0.3240$ W.

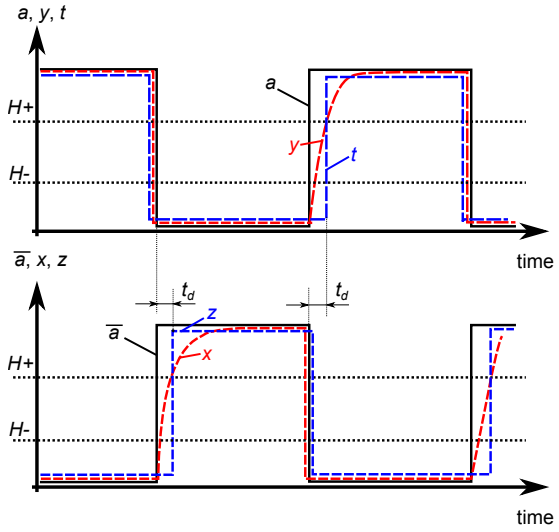


Figure 3.58: Explanation of how the circuit of Fig. 3.57 provides a dead-time.

2. The loss due to the leakage current in the complementary CMOS output stage of the driver chip. This is called the quiescent loss P_Q. It is equal to:

$$P_Q = 2(I_{QH} \cdot \delta + I_{QL} \cdot (1 - \delta))V_{DD} \tag{3.103}$$

with δ the duty cycle, and I_{QH} and I_{QL} the leakage currents during the high, respectively low states of the gate driver. The factor 2 originates from the fact that two drivers are used in the same TC4427 package. For the driver of this Chapter, I_{QH} and I_{QL} are 1.7 mA and 0.18 mA, and δ is 0.5. This gives a loss of $P_Q = 0.0226$ W, which can be neglected with respect to the other losses in the driver.

3. The crossover loss, P_C, due to the fact that the two CMOS transistors of the output stage of the driver chip are both on at the same time. This loss is equal to the product of the cross-conduction constant, listed in the datasheet of the driver chip, and the gate voltage and switching frequency:

$$P_C = f_s \cdot CC \cdot V_{DD} \tag{3.104}$$

For the TC4427 chip, with two drivers in the same package active, and for the operational parameters of this design, $CC = 5.3 \cdot 10^{-9}$ A.s. Thus, $P_C = 0.1908$ W

The total gate-driver loss is $P_R + P_Q + P_C = 0.3240 + 0.0226 + 0.1908 = 0.5374$ W. A PDIP-package is chosen to accommodate for this loss. The thermal resistance between junction and ambient is $R_{JA} = 125$ K/W. Therefore, a loss of 0.5374 W

will cause the junction to heat up to 67 °C above ambient temperature. This is still acceptable. In comparison, for a TC4422A-driver chip, I_{QH} and I_{QL} are 200 and 60 μA, and $CC = 7 \cdot 10^{-8}$ As. Thus, $P_R = 0.324$ W, $P_Q = 0.0031$ W, and $P_C = 2.52$ W, yielding a total loss of 2.8471 W. A PDIP package doesn't suffice for this loss; a TO-220 package must be chosen, increasing the size of the gate-driver and adding more parasitics to the design. This is the reason why a TC4427 driver chip is chosen for this project.

The gate driver drives the FQP2N60 MOSFET. The gate charge for $V_{ds} = 325$ V, $I_{ds} = 3$ A, necessary to switch the gate between 0 and 12 V is 9 nC. The average current the gate-driver should deliver at a switching frequency of 3 MHz is therefore $(9 \text{ nC}) \cdot 3 \cdot 10^6$ Hz $= 27$ mA. The TC4427 gate-drive chip can easily handle this average current.

In Fig. 3.59, a picture of the realized gate-driver is shown. In Fig. 3.60, the low- and high-side gate-to-source signals are shown when the gate-driver operates at 3 MHz, without driving any transistors The rise time of the signals is 7.4 ns and the fall time is 7 ns.

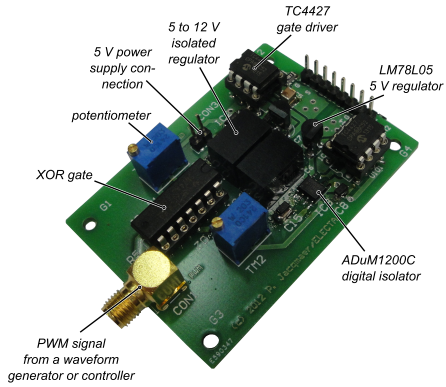


Figure 3.59: Picture of the realized half-bridge gate-driver.

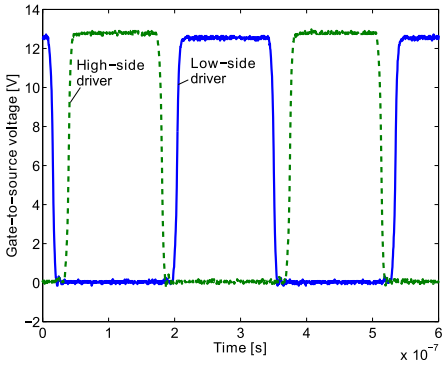


Figure 3.60: Gate-to-source voltages of the high-side and low-side drivers, operating unloaded, at 3 MHz.

3.8 Simulation of the LLC-converter

3.8.1 PSpice simulation model

The LLC-converter is simulated with the Spice model depicted in Fig. 3.62. As can be seen, the dead time, switching frequency and rise and fall times are parameters and the pulse width, delay time and period of the gate signals of

the MOSFETs are deduced from these parameters. The Spice models of the diodes are found on the manufacturer's website. Unfortunately, there is no Spice model available for the FQP2N60 MOSFET. Therefore, the simulation is performed with the STD4NK50ZD-1 MOSFET (cf. Appendix F), of which a Spice model could be found. The equivalent series resistor (ESR) for the coil of the output filter is found in the datasheet, and the parallel capacitance $C8$ is calculated from the self-resonating frequency, listed in the datasheet. Also, the measured transformer model (Fig. 3.43) is combined with the model for the ideal transformer (Fig. 3.49), thereby representing the transformer with a primary coil, two secondary coils and a centre tap. In Fig. 3.61, the gate-drive signals for the two MOSFETs are shown. If the rise times t_{rise} are the same for both the high-side and low-side signals, and the same is true for the fall times t_{fall}, then the period T can be written as:

$$\begin{aligned} T &= t_{rise} + PW + t_{fall} + t_{dead} + t_{rise} + PW + t_{fall} + t_{dead} \\ &= 2t_{rise} + 2t_{fall} + 2t_{dead} + 2(PW) \end{aligned} \tag{3.105}$$

Therefore, the pulse width is equal to:

$$PW = \frac{T}{2} - t_{rise} - t_{fall} - t_{dead} \tag{3.106}$$

and the delay between the two signals is:

$$t_d = t_{rise} + t_{fall} + PW + t_{dead} = T/2$$

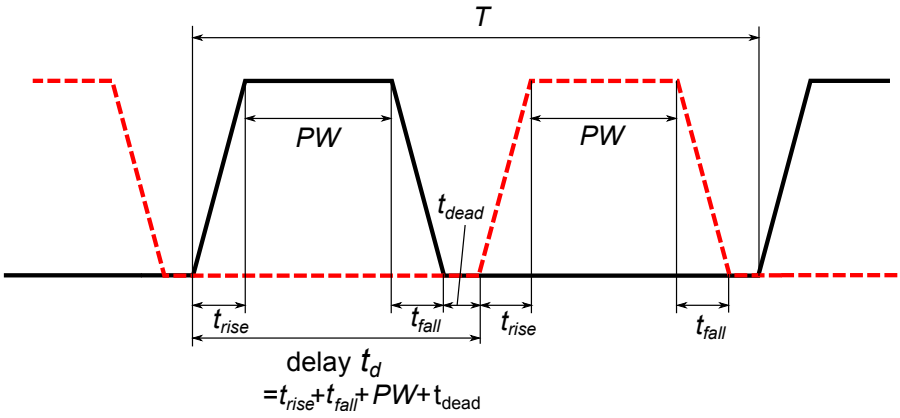


Figure 3.61: Relationship between the different quantities, characterizing the two gate-drive signals.

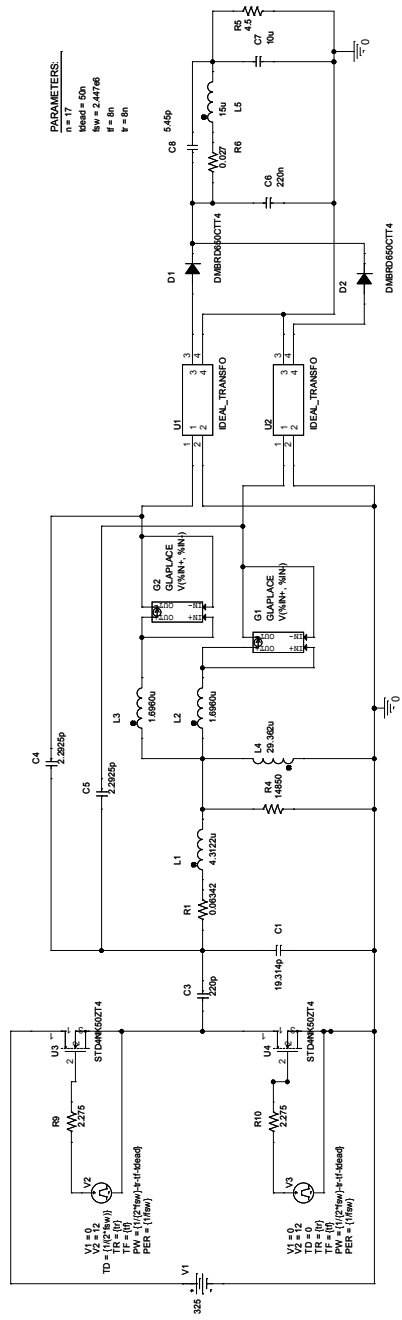


Figure 3.62: PSpice simulation model for the LLC-converter.

3.8.2 Dimensioning the input capacitance of the LLC-converter

The current, flowing through the input DC-source, is simulated in PSpice for the maximum output load of 50 W. It is depicted in Fig. 3.63, when the current is in steady-state. A practical converter needs an input capacitor in order to keep the input voltage more or less constant. There is possibly a long wire between the power supply and the input capacitor, having a lot of inductance and because of this inductance, the power supply cannot deliver a pulsed input current. For this reason, converters with a pulsed input current require input capacitors, being able to supply the pulsed current. Assume that the power supply can only deliver DC-current to the capacitor. When the AC-component of the current flowing out of the input capacitor is positive, the capacitor is discharged and when the AC-component of this current is negative, the capacitor charges again. In the first interval, the input voltage to the converter decreases and in the second interval, it increases again. So, the input voltage has a ripple. In order to determine the necessary value of the capacitor, the charge, drawn out of the capacitor during the first interval is calculated by integrating the positive part of the AC-component of the input current of Fig. 3.63 over time, during one period of the switching frequency. This charge, divided by the capacitance value, is equal to the peak-to-peak voltage ripple. When we allow a ripple of 2 % of 325 V, the necessary capacitance is $C = 8.4$ nF. Ceramic capacitors are chosen because they are fast, and four capacitors of 220 nF each are put in parallel as the input capacitor, thereby overdimensioning the required input capacitance by a factor of about 100. However, the size of the capacitors is still small enough; they are 2220 SMD devices. The GRM55DR72J224KW01L capacitors of 220 nF, 630 V, manufactured by Murata are chosen.

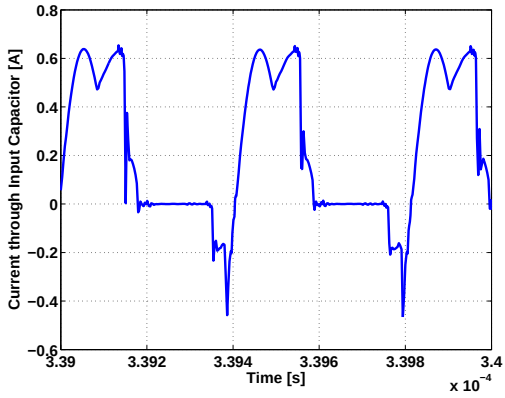


Figure 3.63: Input current of the LLC-converter, at maximum load.

3.8.3 Simulation results

Simulation at heavy ($R_{load} = 4.5\ \Omega$) and light load ($R_{load} = 15\ \Omega$)

The converter is simulated in PSpice for a light load (load resistance is 15 Ω) and a heavy load (load resistance is 4.5 Ω). In order to obtain an output voltage of 15 V, for gate-signals with a rise and fall time of 8 ns, the dead times and switching frequencies have to be set according to Table 3.11. The dead time has to be sufficiently large for ZVS to occur: during the dead time, the drain-to-source capacitance of the MOSFET that is in its off state, discharges so that when the MOSFET turns on again, this occurs at zero voltage.

In Fig. 3.64, the voltage at the half-bridge midpoint, that is the voltage at the input of the resonant tank, is shown, together with the voltage across the series-resonant capacitor for both heavy and light load. It can be seen that the capacitor has to withstand at least approximately 390 V. Also - but this is not shown on the Figure - it was checked that the input voltage of the transformer is purely AC, in order not to saturate the transformer.

Fig. 3.65 shows the voltage across the low-side transistor U4 (cf. Fig. 3.62), the current through it and the gate-to-source signal that drives U4, both for the heavy load and for the light load. When the gate signal goes up, U4 is turned on, and because $V(U4)$ is zero at this instant, the converter realizes ZVS. At turn-off, the voltage is not zero, but this not a problem: the turn-off switching energy is stored in the output capacitor of the MOSFET or flows via the resonant tank towards to output, but is not lost. This is shown in Fig. 3.66. There, the instantaneous power [W or VA] of the MOSFET U4 is shown. The area under the positive peak, indicating that power flows to U4, to charge its output capacitor C_{oss}, is *almost* as large as the area under the negative peak, where this energy is released and flows towards the source or the load. The difference is positive and is 0.65 W for the heavy load condition. At turn on, the energy stored in the MOSFET's output capacitor is dissipated in the on-resistance if there is a non-zero voltage across it. By making the voltage zero, this dissipation is avoided. The resonant tank current is also calculated, with the FHA-assumption, at 2.447 MHz, for the maximum load. A value of 0.71 A is obtained, corresponding well with the simulated value shown in Fig. 3.65.

The output voltage and current are shown for both loads in Fig. 3.67. Zooming in on the output voltage, a steady-state peak-to-peak ripple of 1 mV for the light load and of 3 mV for the heavy load can be noticed, easily fulfilling the requirements of 30 mV and 100 mV respectively.

Fig. 3.68 shows the magnetization current in the transformer and the current through the series-resonant capacitor C_{sr} for the two load conditions. The lighter the load, the more equal both currents become.

The input powers, output powers, core losses and efficiencies are depicted in Fig. 3.69. The efficiency is 86% at heavy load and is 77.5% at light load.

The voltage across an output rectifier diode is shown in Fig. 3.70. It can be seen that the diode has to be able to block twice the output voltage, $2 \times 15 = 30$ V. Also, a current peak of 9 A at heavy load has to pass through the diode for a short period of time.

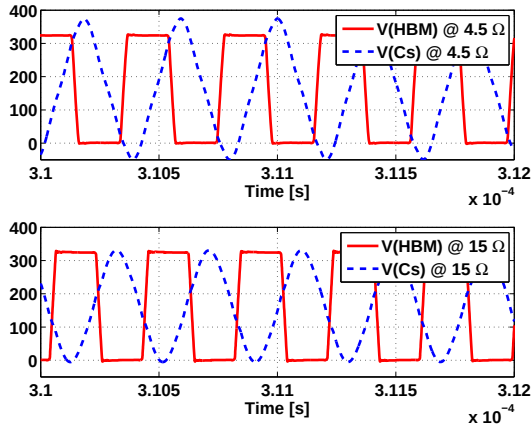


Figure 3.64: Voltage at the half-bridge midpoint and across the series-resonant capacitor $C_{sr} = C3$.

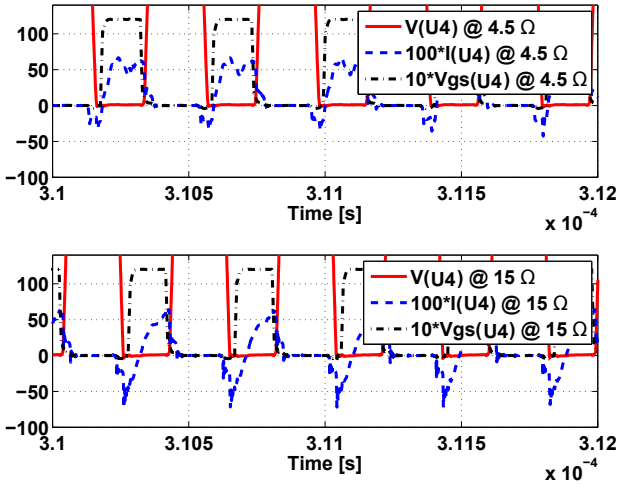


Figure 3.65: Voltage across the low-side MOSFET U4, current through it (multiplied with a factor 100), and the gate-to-source signal driving U4 (multiplied with a factor 10).

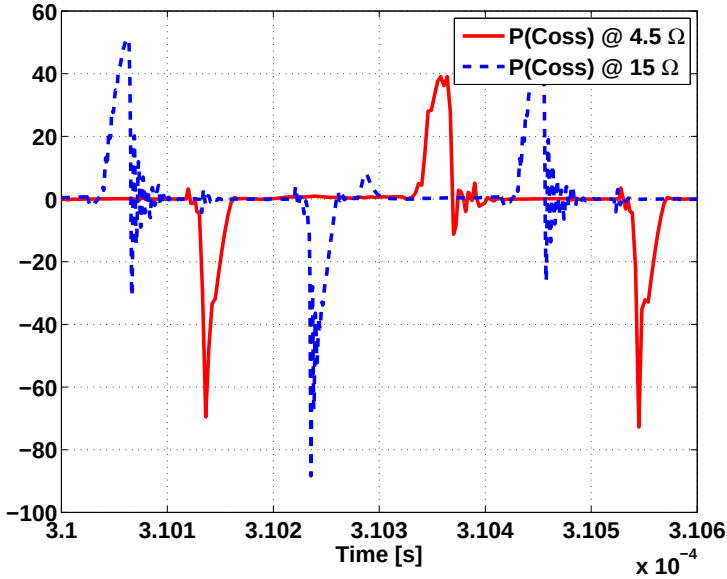


Figure 3.66: Instantaneous power towards the low-side MOSFET U4.

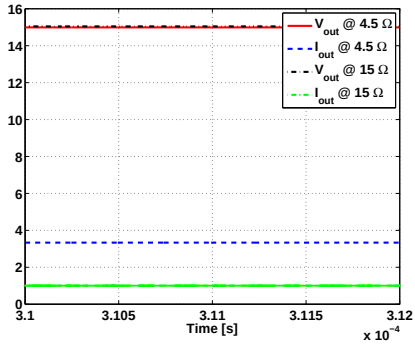


Figure 3.67: Output voltage and current.

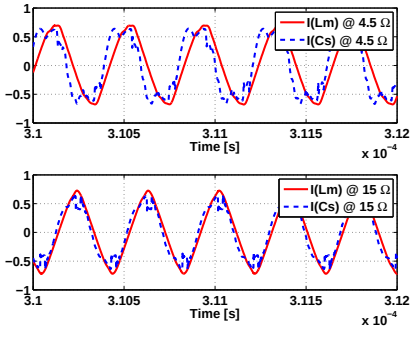


Figure 3.68: Magnetization current through $L_m = L4$ and current through the series-resonant capacitor $C_s = C3$.

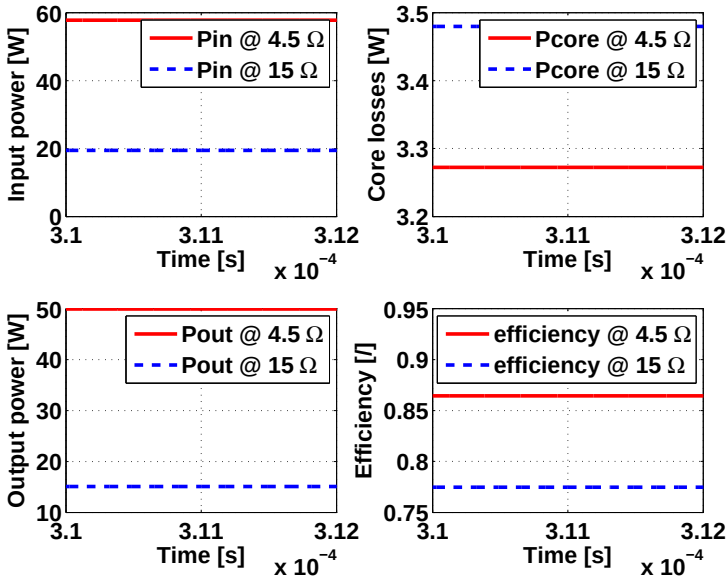


Figure 3.69: Input power, output power, core losses, efficiencies.

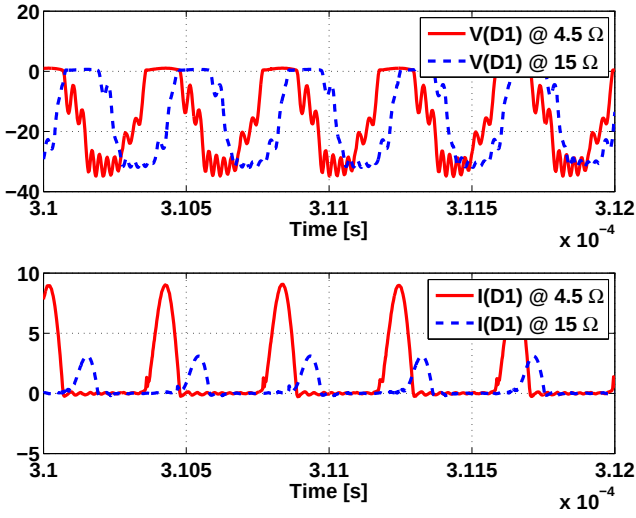


Figure 3.70: Voltage across and current through an output diode.

Simulation at no load

At no load, the output voltage can be regulated to 15 V, but with a dead time of 50 ns, the switching frequency has to increase to 3.927 MHz. Here, ZVS is not obtained because the current in the resonant tank is not sufficiently high to discharge the output capacitance of the MOSFETs during the dead time period. ZVS can be achieved however by increasing the dead time to 73 ns as was discovered by simulation. Then, the output voltage decreases, so the necessary amplification should increase. Therefore, referring to Fig. 3.25, the frequency has to decrease. It is found that a frequency of 3.485 MHz, with this dead time, achieves ZVS and an output voltage of 15 V.

Table 3.11: Gate-drive signals for regulating the output voltage to 15 V.

R_{load} =	4.5 Ω	15 Ω
t_{rise} [ns]	8	8
t_{fall} [ns]	8	8
t_{dead} [ns]	50	50
f_s [MHz]	2.447	2.559

Simulation at low load and low frequency

Care must be taken when the converter is operated at low load, i.e. $R_{load} = 15\,\Omega$ and low frequency, i.e. 2 MHz. A simulation in PLECS [PLEC] is done, based on the model of Fig. 3.62. It is seen that the series capacitor has to withstand a peak voltage of more than 1100 V, that the output diode has to withstand a little bit less than 110 V (the MBRD650CTG diode has a breakdown voltage of 50 V) and that the inner output capacitor is subjected to 56 V (the chosen capacitor can only withstand 50 V). It must therefore be avoided to operate the converter at these conditions.

3.8.4 Simulated efficiency and losses

The simulated efficiency of the converter was stated previously and is 86% for a load of 4.5 Ω. Therefore, there is a total absolute loss of 8.14 W. The distribution of the losses over the different elements is shown in Fig. 3.71. It can be seen that the losses in the ferrite core of the transformer constitute the major part of the losses. Secondly important are the losses in the output diodes. It thus makes sense to consider an air-core for the transformer and also optimize the choice of the output diodes. The simulated core losses are 3.2 W, but the Steinmetz formula for 3F4 and the RM8/I core data (Fig. 3.32) predict core losses of about 1.4 W at 3 MHz. It can therefore be concluded that the PSpice

model of the core losses, a simple shunt resistor, is not accurate, but simply gives an idea of the magnitude of the core losses. A method to determine the loss distribution experimentally of the individual components in a converter is given in [Visn 07].

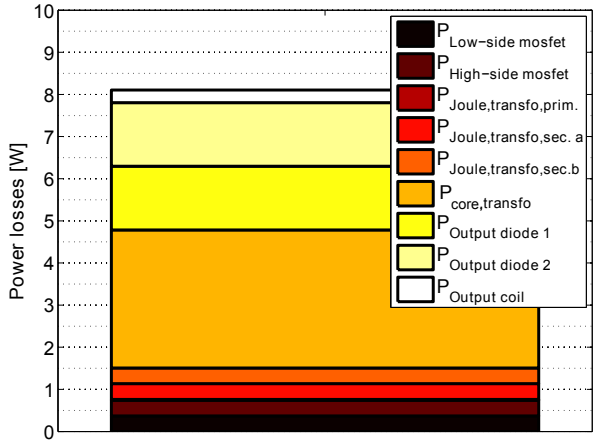


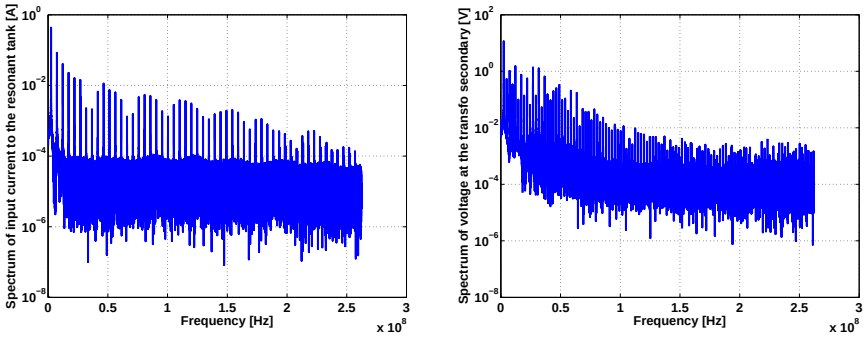
Figure 3.71: Distribution of the losses in the LLC-converter at maximum load.

3.8.5 Verification of the validity of the First Harmonic Approximation assumption

To test the First Harmonic Approximation, which is an approximation that is frequently used in previous Sections to determine the equivalent AC resistance, and which is used for calculating the amplification curves and the frequency region where ZVS is obtained, the input current of the resonant tank and the voltage at the output of the transformer are simulated for the maximum load, 50 W. The spectrum of these signals is determined and shown in Figs. 3.72a-3.72b. Logarithmic scales are used for the ordinate axes, but the fundamental frequency component is by far the most important. The total harmonic distortion is calculated:

$$THD = \frac{\sum_{i=2}^{\infty} X_i^2}{X_1^2} \tag{3.107}$$

with X the current or voltage and X_i its ith frequency component. The THD is 5.9 % for the resonant tank current and is 6.49 % for the transformer output voltage. Therefore, these waveforms are almost perfectly sinusoidal, and the FHA can accurately be made.



(a) Resonant tank input current.

(b) Transformer output voltage.

Figure 3.72: Frequency content of the input current of the resonant tank and the transformer output voltage at maximum load.

3.9 Construction and testing of the LLC-converter

The LLC-converter is built and tested. It was observed that the capacitance of ceramic capacitors decreases a lot with the voltage [Volt 12][Prym 08]. It is therefore possible that, when using ceramic capacitors for the series resonant capacitor, the value of the capacitance does not correspond at all with the value of 220 pF with which the simulations are done. Film capacitors do not have this disadvantage to the same extent as ceramic capacitors. The polypropylene WIMA FKP2O102201D00JSSD capacitors of 220 pF and 1000 V were chosen for the series-resonant capacitor.

The converter is measured with the setup of Fig. 3.73. It consists of a Rigol DG1022 arbitrary waveform generator, a Delta Elektronika SM660-AR-11 power supply, a Topward Electric Instrument TPS-4000 power supply which is used to generate 5 V for the gate-driver, a MetraHit 16S True RMS multimeter to measure this voltage and the output voltage and a Tektronix TDS5054 oscilloscope (500 MHz, 5 GSa/s). The Tektronix differential P6250 probe (500 MHz) and the high-voltage probe P5100A (500 MHz) are used to measure the voltage signals.

For a low load, corresponding to a load resistance of 15 Ω, the drain-to-source voltage and scaled versions of the gate-to-source voltage of the low-side MOSFET and of the resonant current through the tank are shown in Fig. 3.74. It can be seen that ZVS during switching-on is attained as the drain-to-source voltage has reached its low level when the gate signal goes up and exceeds the threshold voltage (between 2 and 4 V for the FQP2N60C MOSFET). The resonant tank current is of an inductive nature. The switching frequency is 2.22 MHz. As can

be seen in Fig. 3.75, the output voltage is almost 15 V.

However, it was observed that for high loads, it was more difficult to attain ZVS, as the theory of Section 3.6.2 predicted. At a load resistance of 4.5 Ω, ZVS could not be reached. The minimal load resistance at which ZVS could be observed, is 5.65 Ω. For this load, the drain-to-source voltage and scaled versions of the gate-to-source voltage of the low-side MOSFET and of the resonant current through the tank are shown in Fig. 3.76. Again, ZVS can be observed here, as the drain voltage reaches its low value when the gate voltage goes up and reaches the threshold voltage value of the FQP2N60C MOSFET. The switching frequency is 2.5 MHz and the dead time, measured on the gate-to-source voltage signals between the gate threshold levels, is 70.0 ns. The output voltage behaves as in Fig. 3.77. An output voltage of 15 V could not be attained. The control frequency region in which the converter operates in ZVS, is the interval [2.4, 2.6] MHz, and is thus 200 kHz wide. It is not wide enough to allow the converter to have 15 V output voltage. This is also illustrated by the curves of Fig. 3.78, where the output voltage is plotted as function of the switching frequency, for different load values and dead times (Table 3.12). This Figure should be compared with the theoretical curves of Fig. 3.25.

In Fig. 3.79, the charge is measured which is stored in the output capacitor C_{oss} of the low-side MOSFET and evacuated from the output capacitor of the high-side MOSFET. The sum of these two charges is Q. It is also the integral of the resonant tank current between the moment that the gate-to-source threshold voltage is reached and the moment that the drain-to-source voltage reaches the source voltage of 325 V. Numerically integrating the resonant tank current between these two time instances gives a charge of $Q = 39.37$ nC. However, integrating the curve for C_{oss}, which is given in the datasheet of the MOSFET, between 0 and 325 V, and multiplying it with two[3], gives a charge of 23.402 nC. This discrepancy can explain why it is not possible to reach ZVS at a load of 4.5 Ω, while in Section 3.6.2 it was predicted that it was possible.

The efficiency is measured for the load resistance of 5.65 Ω. The output power is 52.85 W. The output voltage is 19.14 V and the output current is 2.76 A. The input power is 62.78 W, at a voltage of 317 V and a current of 0.19799 A. This gives an efficiency of $52.85/62.78 = 84.2$ %. This corresponds well with the value of 86 %, predicted by the simulations (Section 3.8.3). The difference can be explained by the simplified simulation model of the core losses (one resistance), a feature which can be improved in a future work.

In Fig. 3.80, the measured output voltage for a load of 5.65 Ω and duty cycle DT4 is compared with the theoretically predicted output voltage, where the

[3]Multiplying with 2 because the output capacitance of one MOSFET is discharged with a certain charge and the output capacitance of the other MOSFET is charged with the same charge.

model of Fig. 3.62 has been used, when the FHA is assumed and when there is no dead time.

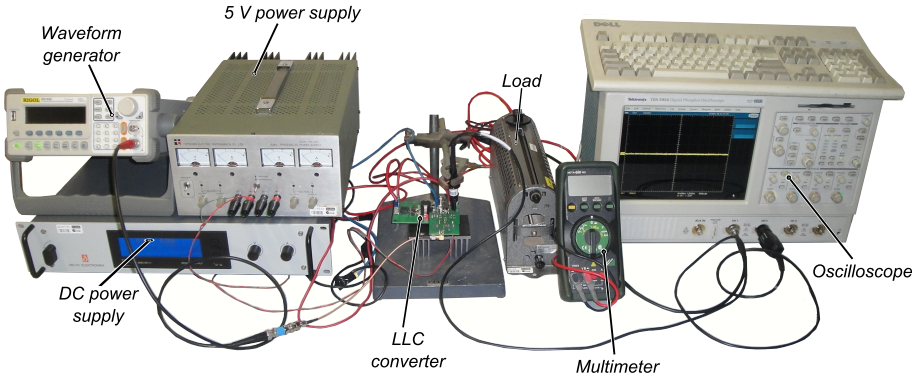


Figure 3.73: Test setup.

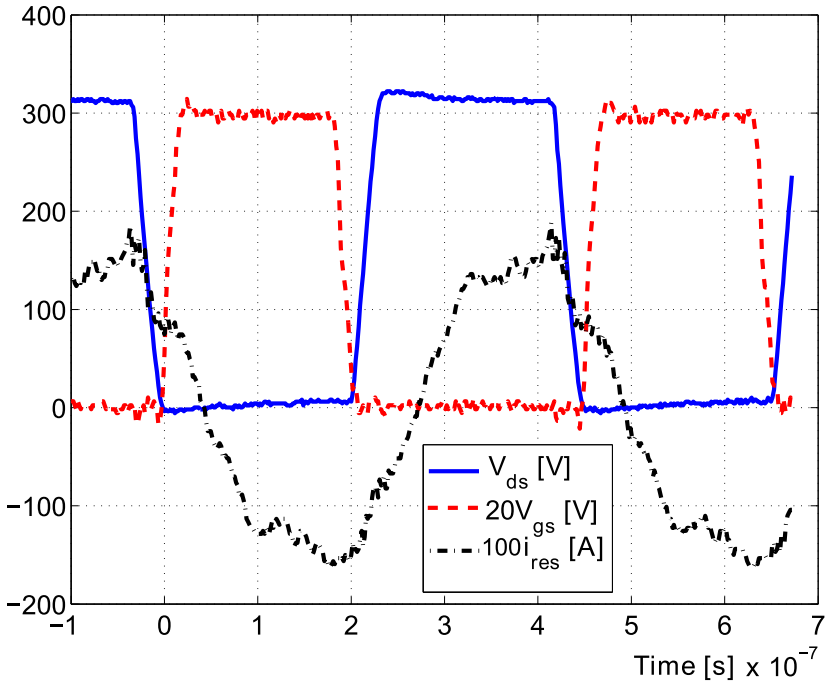


Figure 3.74: Gate-to-source voltage of the low-side MOSFET (multiplied with 20), drain-to-source voltage and resonant tank current (multiplied with 100) at light load, 15 Ω.

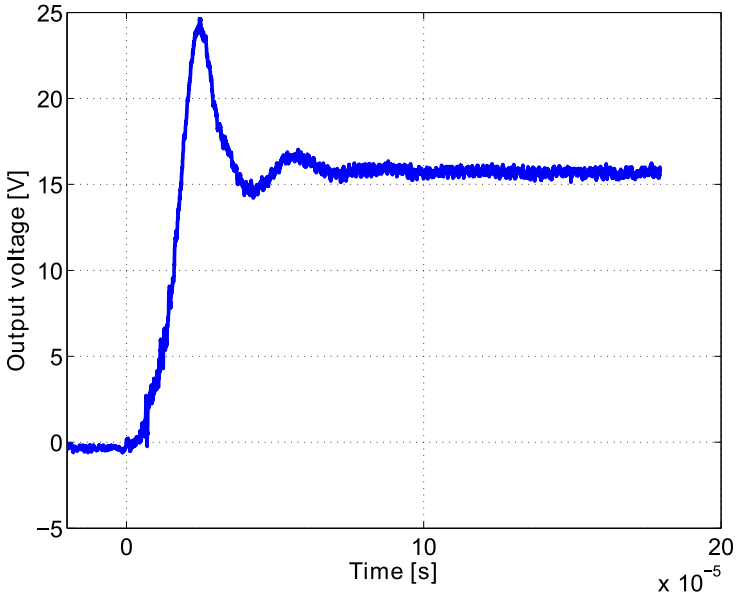


Figure 3.75: Output voltage at light load, 15 Ω.

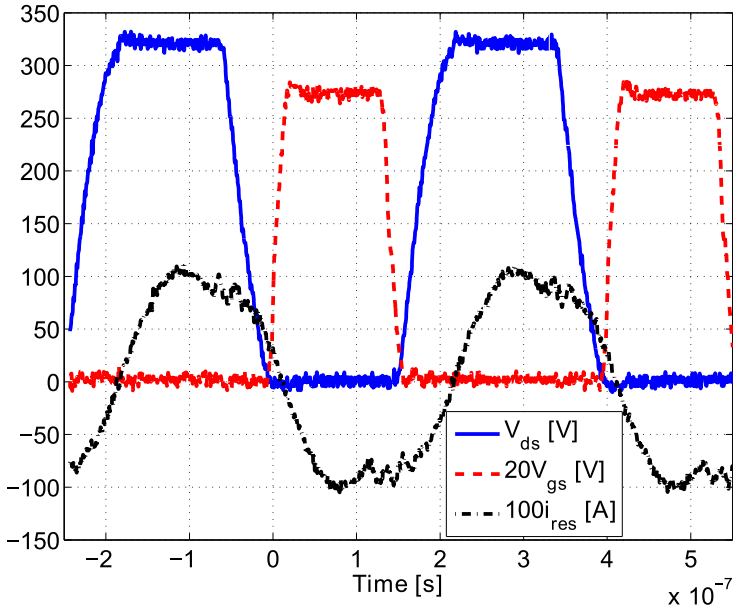


Figure 3.76: Gate-to-source voltage of the low-side MOSFET (multiplied with 20), drain-to-source voltage and resonant tank current (multiplied with 100) at heavy load, 5.651 Ω.

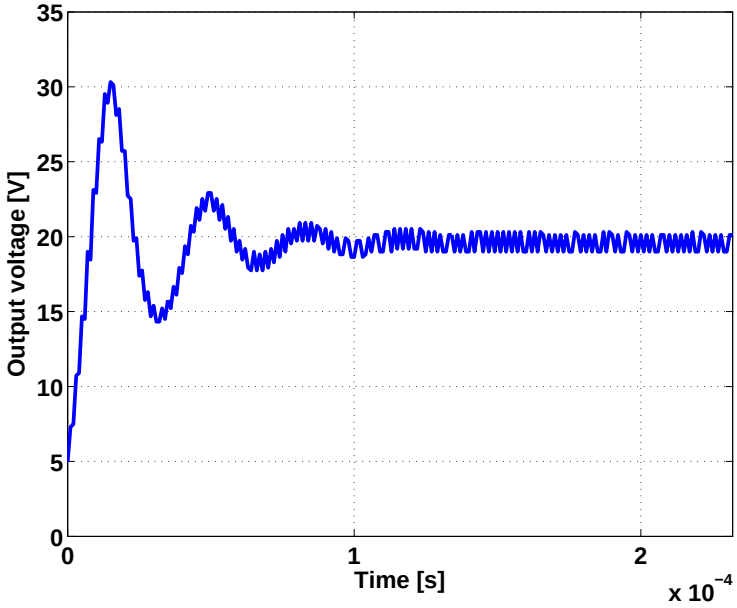


Figure 3.77: Output voltage at heavy load, 5.65 Ω.

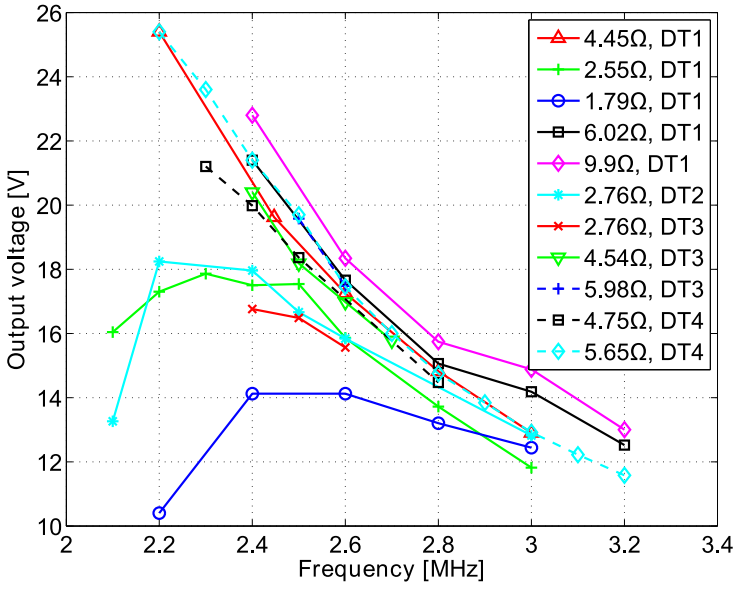


Figure 3.78: Output voltage in function of switching frequency for several load resistances and dead times.

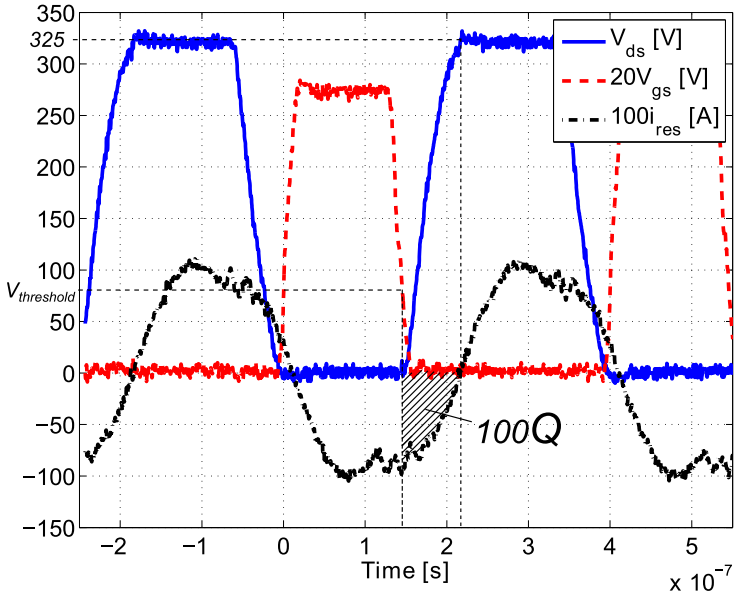


Figure 3.79: Calculation of the charge, needed to charge and discharge the output capacitors of the two MOSFETs, at load 5.651 Ω.

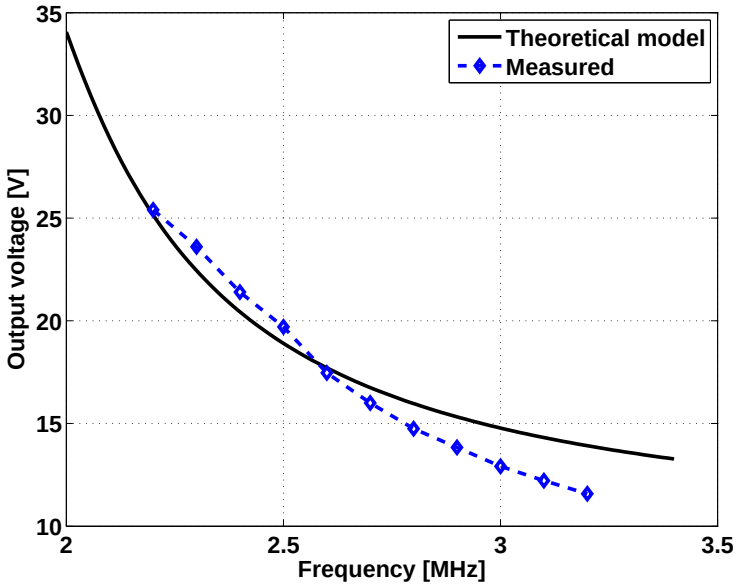


Figure 3.80: Comparison of the measured output voltage for a load of 5.65 Ω and a duty cycle DT4 with the theoretically predicted output voltage.

Table 3.12: Dead times used in the experiments.

DT1	DT2	DT3	DT4
18.1 ns	57.1 ns	30.0 ns	70.0 ns

3.10 Conclusion

This Chapter researches a second possibility to achieve high switching frequencies in power converters. Resonant switching strategies can be employed to decrease the switching losses. The switching losses are proportional to the switching frequency and hence, for a specific amount of losses, the frequency can be increased in resonant converters with respect to hard-switching converters.

Several multi-megahertz converters presented in literature, are indicated on a map showing the output power versus the switching frequency. Based on this map, specifications for output power and switching frequency are chosen for a DC/DC-convertor which is to be designed and operates with resonant switching strategies. The output specifications are 50 W, 15 V $\pm$100 mV and the minimum switching frequency should be above 2 MHz. Furthermore, the input voltage is 325 V $\pm$10%. The aim of this Chapter is firstly to completely design such a converter, showing all the design stages that such a topology requires and secondly, to completely optimize the chosen components. It is the first soft-switched converter, realized in research group Electa.

The Chapter then continues with the search for a suitable resonant topology. A condition for zero voltage switching (ZVS) is found; ZVS is obtained when the resonant tank is inductive and when the dead time assumes a certain value, located in a specific interval, for which mathematical expressions were found. When the input impedance of the resonant tank is capacitive, zero current switching (ZCS) can be achieved. It is explained why MOSFETs benefit from ZVS operation while IGBTs benefit from ZCS operation. Many different resonant topologies exist: series, parallel and hybrid topologies. In the class of the hybrid-resonant converters, a distinction can be made between LLC-, LCC- and LLCC-converters. For all these types, an equivalent output resistance is calculated, using the First Harmonic Approximation (FHA). The FHA makes use of the fact that the input current to the resonant tank is almost perfectly sinusoidal and calculates the characteristics of the tank with only the first harmonic frequency of the waveforms. This assumption is later in this Chapter checked and verified. The impedance of the resonant tank and the amplification factor are calculated in function of the frequency for all the types of resonant converters. The regions of operation where ZVS and ZCS can be achieved, are indicated in these graphs.

For 50 W, a half-bridge topology is preferred over a full-bridge. Hybrid topologies

offer more degrees of freedom for the design, so they are preferred over serie- and parallel-resonant converters. Finally, an LLC-structure is preferred over an LCC-topology, because the frequency operation interval of an LCC-converter is typically shifted to higher frequencies with respect to that of an LLC-converter, leading to higher losses in the magnetic components. Also, it is easier to incorporate the parasitic components of a transformer in the converter, into the resonant tank of an LLC-converter, than into the resonant tank of an LCC-converter.

Different magnetic materials are researched next, suitable for high-frequency operation. Requiring that the material should have low core losses and should be easily available, the 3F4 ferrite material from Ferroxcube is chosen. All cores types from Ferroxcube of a specific estimated size, available in 3F4-material, are assessed and the one with the lowest core losses, combined with the highest series resonant capacitor is chosen. This is a Planar E PLT32/20/3/R core, but the next best one, RM8/I, is chosen for the final design because of ease of fabrication.

In a next step, the optimal parameters of the resonant LLC-tank and an optimal transformation ratio are determined. A parametric sweep is done for different transformation ratios where the magnetization inductance, the primary leakage inductance and the series resonant capacitance are varied. A transformer is constructed and its equivalent high-frequency lumped model is determined with measurements. For the secondary winding resistance, an accurate frequency-dependent model is used. Also the feasibility of the use of an air-core transformer is investigated, and it is seen that actually, even for the frequencies of this work, an air-core transformer is a valid alternative. However, this is true only if the magnetic coupling between the primary and secondary coils is not negatively influenced by the lack of a magnetic core. For that reason, because it was feared that there would be too much leakage, the ferrite core is kept in the design.

A discussion follows, regarding the choice of the MOSFETs suitable for this project, the design of the output rectifier and the output CLC-filter.

This Chapter next presents a half-bridge gate-driver, suitable for producing multi-megahertz signals with a duty ratio of 50 % and offering the possibility of adjusting the dead-time.

The converter is then simulated in PSpice, and ZVS is observed. The frequency settings are determined to obtain 15 V at the output for two load conditions. The efficiency is calculated at heavy and light load. An efficiency of 86% is predicted at 50 W output power and the efficiency at an output power of 15 W is 77.5%. The distribution of losses in the converter is calculated and the major part of the losses are generated in the magnetic core and the output diodes.

The converter is next built and tested. ZVS is observed at low load, but cannot be reached at high load. The minimum output resistance at which ZVS can

be attained is 5.65 Ω. At this load, the frequency control region where ZVS is present, is then only 200 kHz wide and an output voltage of 15 V cannot be reached. The efficiency at this load is 84.2 %, which is quite good as compared to the efficiencies of the state-of-the-art multi-megahertz converters of Table 3.2. Curves of the output voltage versus the frequency are measured and compared with the theoretical curves.

4

Modelling Parasitics of Printed Circuit Board Tracks

When semiconductor technology advances and power transistors switch on or off in a shorter period of time than they used to, new problems arise, of which power electronics engineers should be aware already in the design phase. That is, when a switching transient takes place in a power electronic converter, magnetic energy, stored in the inductive printed circuit board (PCB) tracks and in inductive parts of the semiconductor components or passive elements present in the power circuit, is partly dissipated and partly transformed into electric energy which is stored in capacitive circuit elements. This transfer of energy occurs in an oscillating manner, going back and forth between inductive and capacitive elements, and changes in intensity, causing voltage and current fluctuations (ringing) across and through circuit components, subjecting them to a higher electrical stress. The faster the transistor switches the more problematic this is as for a specific circuit topology, the same amount of energy has to be transferred in a shorter period of time, thus inflicting oscillatory waveforms with higher amplitudes and more electrical stress on circuit components.

Not only are the power semiconductors subject to a higher electrical stress, the aforementioned oscillations cause unwanted radiation as well, disturbing the electromagnetic environment of the circuit and causing radiation losses. This particular phenomenon will be discussed in the next Chapter. Chapter 4 quantizes the ringing, overshoot, crosstalk and signal integrity issues in fast power converters. Also, because of a possible higher voltage across the switch just before it switches to the on-state, the problem of charge trapping, as discussed in Chapter 2, can be more severe and can cause more losses than in circuits where voltage ringing is not present.

Parts of the PCB-tracks store magnetic or electric energy. Hence, they contribute to the problem of ringing. It is therefore important that a method is devised to accurately model the parasitic energy storage possibilities of the PCB-tracks. The purpose of this method is to predict to what extent a specific circuit design will show ringing and overshoot.

The freeware software programmes FastCap [Nabo 92] and FastHenry [Kamo 30] are used to create a model of the PCB-tracks. This model consists of resistances, self- and mutual inductances and self- and mutual capacitances. It can be easily loaded into a circuit simulator such as Spice, together with models for other components such as the diodes, transistors, coils and capacitors. This way, the power electronic circuit can be simulated in the time- or frequency-domain, returning electrical currents and voltages typically being subject to effects of ringing and overshoot.

4.1 Introduction

Recently, the power electronics community is becoming more and more interested in using wide-bandgap semiconductors as building material for power switches. These materials exhibit advantageous features such as diminished dimensions for the same blocking voltage with respect to silicon components. Hence, devices, made from wide-bandgap materials, are faster than silicon devices and can operate at increased switching frequencies. However, when frequencies increase and rise or fall times decrease, the layout of the circuit, typically implemented as a printed circuit board, starts to play an important role in the behaviour of voltages and currents because unwanted parasitics due to the geometry of the copper tracks of the PCB are more outspokenly present at higher frequencies. Voltages and currents will show oscillations and sometimes huge over- and undershoots due to these parasitics and will subject the active switching components to more electrical stress, which can possibly damage them or reduce their life span ([Oh 00], Section 5.14). Also, it is possible that the effects of the parasitics distort the waveforms so much that the correct operation of the circuit deteriorates or even ceases. Therefore, it is highly advisable to

have a method for modelling the parasitics, so that one can quickly see what their effect is on the circuit's waveforms.

In this Chapter, a method is presented to extract an RLC-equivalent network, representing the PCB-tracks. This is done using the freeware software tools FastHenry and FastCap, extracting respectively the resistance and inductance matrix, and the capacitance matrix from a circuit consisting of conductors and (for FastCap) one or more dielectric volumes. FastHenry and FastCap are developed at the Computational Prototyping Group of Massachusetts Institute of Technology (M.I.T.) by Jacob White, Mattan Kamon and their colleagues. They calculate the R-, L- and C-matrices under the quasi-static assumption and use the multipole expansion technique for speeding up the calculation process [Kamo 30][Nabo 92]. The method of this work produces an electric model for the PCB-tracks, which can be inserted in Spice, together with the other elements of the power electronic converter, such as coils, diodes, MOSFETs, IGBTs.... Also other circuit simulators can be used but in this work, Spice is chosen.

The method is explained with an example, first cited in [Rueh 74], where a sort of resistance-divider circuit, subjected to a step voltage, is modelled. The circuit is built and measurements are compared with the simulation results. In a next Section, the method is applied to a step-down power electronic circuit, which is called a reversed buck circuit, because the switch has its source connected to the ground, making it possible to use a non-isolated gate-driver. Again, measurements and simulation results are compared and show a good agreement, indicating that the method of this work produces accurate results. The method is next applied to a long transmission line where the wire dimensions have a large aspect ratio. Furthermore, it is applied to the problem of the two-capacitor paradox. However, as will be explained, this is a badly conditioned problem which is hard to calculate numerically. To demonstrate its full-wave properties, the method of this work is next applied to calculate the currents along a transmission line, operating at high frequencies. In the last Section of this Chapter, a freeware software programme, PCBParC, is presented, implementing the method of this work. It can be freely downloaded from the Internet, and extracts a Spice-subcircuit modelling the parasitics of the PCB-tracks of power converters. The possible PCB-geometries which the programme can process, must have PCB-tracks with a rectangular cross-section, on a single-layer dielectric board, where the tracks are parallel or orthogonal to each other. Because the programme makes use of FastHenry, the skin and proximity effects are taken into account.

4.2 Modelling techniques

Accurate electromagnetic modelling of PCB-tracks has already been researched at Electa by dr. ir. Bruno Bolsens [Bols 05]. He used the Moment Method with a thin-wire assumption [Harr 68] [Gibs 07] in order to model cylindrical wires connected to electrical circuit components. Advantages of his technique are the following:

- The Method of Moments (MoM) is a full-wave electromagnetic method, meaning that it solves Maxwell's equations without neglecting terms such as the term of the displacement current in Ampère-Maxwell's equation or the $\partial\vec{B}/\partial t$-term in the Faraday-Lenz equation as is done in quasi-static methods.
- It is based on solving equations in the frequency-domain. Then, the steady-state solution is calculated and the (often unimportant) transient start-up phenomenon is omitted. The Method of Moments typically is a frequency-domain method, although recently there are attempts to implement a time-domain version of the method [Ghaf 09].
- Furthermore, because the frequency components of the currents through and the charges on the wires are available, the electromagnetic fields, scattered by the electric circuit can be easily calculated. Expressions are readily available for the frequency components of the $\vec{E}$- and $\vec{H}$-field if the sources of these fields, the currents and charges, are expressed in the frequency-domain. This will be shown in the next Chapter.
- Bolsens's method is fast, despite the fact that the Moment Method leads to a dense $N \times N$-matrix if N wire segments are present in the circuit. A finite element method however uses sparse matrices and has typically only elements in the vicinity of the main diagonal.
- Bolsens's method can be universally applied for any kind of power electronic converter.
- The wires can be placed in any geometrical configuration in space. They do not have to lie in a plane and can have all kinds of angles with respect to each other.

However, there are also some disadvantages:

- Bolsens's method only allows cylindrical wires in the structure. PCB-tracks, having a rectangular cross-section, are not allowed. However, there exists an equivalent radius to map each rectangular PCB-track to an

equivalent cylinder [Leon 05]. Bolsens uses the thin-wire approximation for the cylinders which states that the complete current is a line source, located on the axis of the cylinder. Therefore, his method is a 1D-implementation of the Method of Moments. Also 2D- and 3D-versions have been developed in literature.

- In Bolsens's work, the substrate supporting the PCB-tracks, is not modelled. However, there exist Moment Method techniques [Carl 98] which can take a dielectric substrate and even a copper ground plane on the other side of the substrate into account.

- Bolsens only allows ideal switches and diodes. These only operate in two distinct modes: either they conduct with an on-resistance of 0 Ω, or they block the current perfectly and have an extremely high resistance. The operating point changes instantaneously from one mode to the other, because no parasitic capacitances are present. This is an important disadvantage of Bolsens's method. In fact, because there are only infinitely sharp edges of current and voltage, he calculates the worst-case scenario for radiation and overshoot in the waveforms. In reality, the edges are more smooth and radiation and overshoot are more relaxed. Also important to note is that the internal capacitances of power switches and diodes are voltage-dependent. A frequency-domain method typically has a lot of problems to take this voltage-dependency into account.

- Another disadvantage of a frequency-domain method with infinitely sharp edges of the current or voltage time-domain waveforms is the fact that the Gibbs phenomenon will be present in the time signals if they are calculated as the inverse Fourier transform (IFT) of the frequency-domain signals. The Gibbs phenomenon states that if there is a discontinuity in the time-domain signal, the inverse Fourier transform of the Fourier transform of this time signal will show oscillations around the discontinuity. These oscillations will remain, even if one takes an infinite amount of terms in the (inverse) Fourier series. The height of the oscillation bump closest to the discontinuity is approximately $0.09(f(t_0+) - f(t_0-))$, where $f(t)$ is the time signal, t_0 is the abscissa where the discontinuity occurs and $f(t_0-)$ and $f(t_0+)$ are the left and right limits of f for $t \to t_0$ respectively. A solution can be to use a filtering window (Hamming, Hanning, Kaiser, Blackman...) [Nuta 81] or Lanczos coefficients in the (inverse) Fourier series [Duch 79], but all these solutions decrease the slope of the voltage or current signal edges and in order to make them steeper again, a large nuber of harmonics should be taken into account.

- Bolsens places the charges as localized point charges on the extremities of the wire segments. One should notice that the electric field, of which the magnitude decays as $1/R$, $1/R^2$ or $1/R^3$ around the charges, with R the distance from the charge, becomes infinite at the position of the charge.

> One should therefore never calculate the field very close to a charge, for this reason. The method of Bolsens thus only gives good results for the electric field at a sufficient distance of each charge.

Because of these disadvantages, it is decided to use a time-domain method, where a commercial circuit simulator will solve the component equations in order to accurately simulate the physical behaviour of switches and diodes. Then, the Gibbs phenomenon will not be present because there will not be any infinitely sharp edges anymore. Furthermore, the voltage dependency of the internal capacitances of semiconductors can be taken more easily into account in the time-domain. In the next Sections, it will be explained that FastHenry and FastCap will be used to calculate the resistances, partial inductances and capacitances. FastHenry is especially useful for metallic conductors with a rectangular cross-section. FastCap allows the presence of one or more dielectric substrates. However, these programmes are based on a quasi-static assumption, not allowing wave propagation effects. Therefore, for very high frequencies, the method outlined in this work will produce results that are not correct if the segmentation of the tracks is too coarse. However, with a sufficiently small segmentation, the method can also solve wave propagation problems. At Electa, there is also other work in progress [Zwys 12] where the S-parameters of the PCB-tracks are extracted with a commercial simulation software. A circuit solver is designed in that work, using the S-parameters and accounting for the internal capacitances and other internal parasitic elements of semiconductors, so that full-wave calculations are performed in the frequency-domain.

4.3 Partial Element Equivalent Circuit models

For a system of K conductors, constituting an electric circuit, present in an isotropic and homogeneous medium with permittivity ϵ and permeability μ, the Electric Field Integral Equation (EFIE) can be written. The k^{th} conductor is segmented in Q_k surface cells (also called capacitive subdivisions) with surface S and $N_{\gamma,k}$ volume cells (also called inductive subdivisions), associated with direction γ ($= x$ or y or z), having a volume V. The current density $\vec{J}$ and charge density ρ are sought as linear combinations of unit pulse functions and the EFIE is subsequently discretized. Galerkin weighing is then applied in order to find a solution for the unknown coefficients of the linear combination. With A_γ the area of the cross-section of a conductor, perpendicular to direction γ ($=x$ or y or z), with $\vec{r}$ the position vector of the observation point, with $\vec{r'}$ the position vector of a source point, with $R = |\vec{r} - \vec{r'}|$ and with t_n and t_m retarded

times, the system of discretized EFIEs is:

$$\frac{I_{\gamma,m,l}(t)l_m}{A_{\gamma,m,l}\sigma}+$$

$$\sum_{k=1}^{K}\sum_{q=1}^{Q_k}\frac{1}{4\pi\epsilon}\left[\left(\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{|\vec{r^+}-\vec{r'}|}dS'_{q,k}\right)-\left(\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{|\vec{r^-}-\vec{r'}|}dS'_{q,k}\right)\right]+$$

$$\sum_{k=1}^{K}\sum_{n=1}^{N_{\gamma,k}}\frac{\mu}{4\pi}\left[\frac{1}{A_{\gamma,n,k}}\frac{1}{A_{\gamma,m,l}}\int_{V_{\gamma,m,l}}\int_{V_{\gamma,n,k}}\frac{\frac{\partial}{\partial t}I_{\gamma,n,k}(t_n)}{R}dV'_{\gamma,n,k}dV'_{\gamma,m,l}\right]\approx l_m E_{i,\gamma,m,l}(t) \tag{4.1}$$

The derivation is given in Appendix H. It can also be found in references [Rueh 74] and [Ekma 03], but there less intermediate calculation steps are given. The method and its derivation already exist and are not new contributions of this work; however the combination of this method with FastHenry and FastCap and the use of a circuit solver such as Spice which also can solve full-wave problems, are new. In (4.1), $\vec{r^+}$ and $\vec{r^-}$ are the position vectors to the points on a surface, that is obtained from the corresponding surface of the inductive cell (γ, m, l), by translating it over a distance, equal to half the inductive volume's length, in one direction (for $\vec{r^+}$) or in the opposite direction (for $\vec{r^-}$). This means that the capacitive cells must be translated with respect to the inductive cells. Fig. 4.1 explains this for the partitioning of a plate.

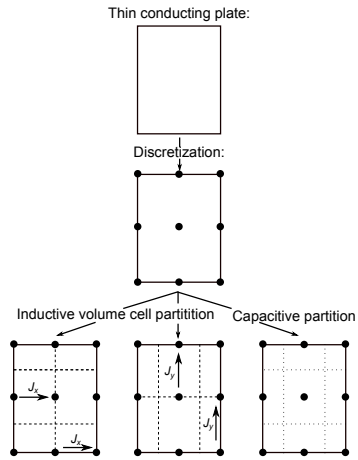


Fig. 4.1: Inductive volume cells and capacitive surface cells. Dark circles represent nodes, dashed lines separate volume cells and dotted lines separate surface cells. Source: [Ekma 03]

4.3.1 Resistive term

The first term of eq. (4.1) represents the resistive voltage drop across the volume cell (γ, m, l). The reason is that it is a current, multiplied with a resistance corresponding to Pouillet's law:

$$R_{m,l} = \frac{l_m}{A_{\gamma,m,l}\sigma} \tag{4.2}$$

The resistive PEEC-model for the volume cell (γ, m, l), connecting nodes i and j is shown in Fig. 4.2. It is simply a resistive element connecting these nodes.

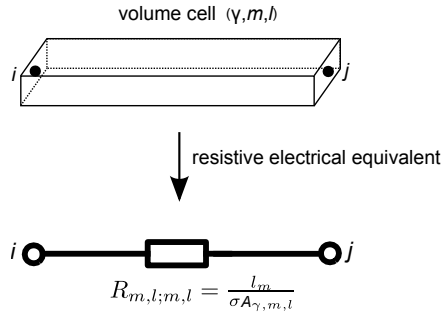


Fig. 4.2: Resistive PEEC-model for a volume cell connecting nodes i and j.

4.3.2 Inductive term

First, rewrite the third term of eq. (4.1). The assumption is made that the current through the cell (γ, n, k) is constant. This assumption neglects the skin-effect and proximity effect which occur in conductors. However, as will be shown later on, the PEEC-technique can be extended so that it is able to cope with the skin-effect. Also, it is assumed that the delay t_n is constant in the double integration. It is approximated as the centre-to-centre delay between the geometric centres of the source cell (γ, n, k) and the observation cell (γ, m, l). With these two assumptions, the time-derivative of the delayed current can be brought outside the two integrals and becomes a true derivative[1]. The third term of (4.1) then becomes:

$$\sum_{k=1}^{K}\sum_{n=1}^{N_{\gamma,k}}\left[\frac{\mu}{4\pi}\frac{1}{A_{\gamma,n,k}}\frac{1}{A_{\gamma,m,l}}\int_{V_{\gamma,m,l}}\int_{V_{\gamma,n,k}}\frac{1}{R}dV'_{\gamma,n,k}dV'_{\gamma,m,l}\right]\frac{dI_{\gamma,n,k}(t_n)}{dt} \tag{4.3}$$

[1]Not a partial derivative anymore

Since

$$Lp_{m,l;n,k} = \frac{\mu}{4\pi}\frac{1}{A_{\gamma,n,k}}\frac{1}{A_{\gamma,m,l}}\int_{V_{\gamma,m,l}}\int_{V_{\gamma,n,k}}\frac{1}{R}dV'_{\gamma,n,k}dV'_{\gamma,m,l} \tag{4.4}$$

is the quasi-static partial inductance Lp between the two cells (γ, m, l) and (γ, n, k) [Paul 10], the third term of eq. (4.1) clearly represents the inductive voltage drop across the cell (γ, m, l):

$$\sum_{k=1}^{K}\sum_{n=1}^{N_{\gamma,k}} Lp_{m,l;n,k}\frac{dI_{\gamma,n,k}(t_n)}{dt} \tag{4.5}$$

The inductive PEEC-model for the volume cell (γ, m, l), connecting nodes i and j is shown in Fig. 4.3. In this Figure, the partial-inductance $Lp_{m,l;m,l}$ represents the self-inductive effect, and the voltage source $V_{m,l}$ represents the mutual inductive couplings between element (γ, m, l) and all the other elements. $Lp_{m,l;n}$ is the mutual partial inductance between volume cells (γ, m, l) and (γ, n). Here, n is a set of two numbers. i_n is the current through volume cell (γ, n). Furthermore, $\tau_{m,l;n}$ is the time it takes for electromagnetic waves to propagate from the centre of volume cell (γ, m, l) to the centre of volume cell (γ, n).

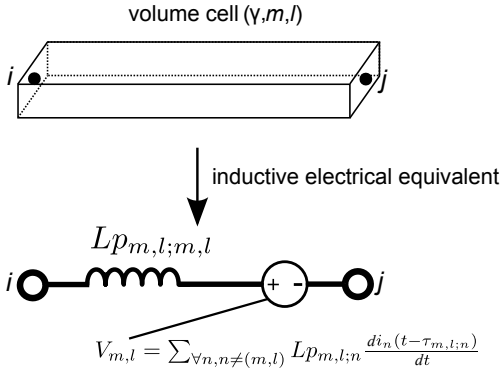


Fig. 4.3: Inductive PEEC-model for a volume cell connecting nodes i and j.

4.3.3 Capacitive term

Denote the charge in Coulombs of surface cell (q, k) by $Q_{q,k} = \rho'_{q,k}S_{q,k}$. With similar assumptions as for the inductive term, namely that the charge is constant over the cell surface[2] and that the delay stays constant in the integration and

[2]Actually, the charge is concentrated more on the surface of a metallic conductor, where the radius of curvature of the surface is largest ([Serw 96], section 24.4)

is equal to the centre-to-centre delay, the second term of equation (4.1) can be written as:

$$\sum_{k=1}^{K}\sum_{q=1}^{Q_k} Q_{q,k}(t_q)\left[p^{+}_{q,k;m,l} - p^{-}_{q,k;m,l}\right] \tag{4.6}$$

with

$$p_{i,j} = \frac{1}{4\pi\epsilon}\frac{1}{S_i}\frac{1}{S_j}\int_{S_j}\int_{S_i}\frac{1}{|\vec{r_i} - \vec{r_j}|}dS'_i dS'_j \tag{4.7}$$

The p's are the static coefficients of potential [Ekma 03]. Therefore, the second term can be seen as the capacitive voltage drop across the volume cell (γ, m, l). Use has been made of surface cells, which are obtained by translating the surface of volume $V_{\gamma,m,l}$ over a vector $l_m/2 \cdot \vec{u}_\gamma$ and over a vector $l_m/2 \cdot \vec{u}_\gamma$ (see Appendix H). With each volume cell correspond therefore two surface cells which are obtained by translating the surface of the volume cell.

The static coefficients of potential are defined as follows. They are elements of the matrix $[P]$. If the charges are collected in a vector $[Q]$ and the voltages in a vector $[V]$, then we have:

$$[V] = [P][Q] \tag{4.8}$$

The inverse equation is:

$$[Q] = [C_s][V] \tag{4.9}$$

where $[C_s] = [P]^{-1}$ is the short-circuit capacitance matrix [Ekma 03]. The capacitive PEEC-model for the surface cell i is shown in Fig. 4.4. In this Figure, the pseudo-capacitance $1/p_{i,i}$ represents the self-capacitive effect and the voltage source V_i represents the mutual capacitive couplings between element i and all the other elements. $V_{C,j}$ is the voltage across the pseudo-capacitance $1/p_{j,j}$, and $\tau_{i,j}$ is the time it takes for electromagnetic waves to propagate from the centre of surface cell j to the centre of surface cell i.

The fact that eq. (4.6) is graphically represented as Fig. 4.4 can be understood as follows. Equation (4.6) is the capacitive voltage drop across inductive cell (γ, m, l). However, as each inductive cell is located between two nodes i and j, node potentials can be assigned. Suppose in the system of conductors, there are N nodes. The potential at node i is according to eq. (4.6) equal to:

$$V_{n,i} = p_{i,i}Q_i + \sum_{k=1,k\neq i}^{N} p_{k,i}Q_k(t - \tau_{i,k})$$

Now let $V_{C,h}$ be the voltage across the pseudo-capacitance $1/p_{h,h}$. We thus have $Q_h/V_{C,h} = 1/p_{h,h}$. Previous equation then becomes:

$$V_{n,i} = V_{C,i} + \sum_{k=1,k\neq i}^{N} \frac{p_{k,i}}{p_{k,k}}V_{C,k}(t - \tau_{i,k}) \tag{4.10}$$

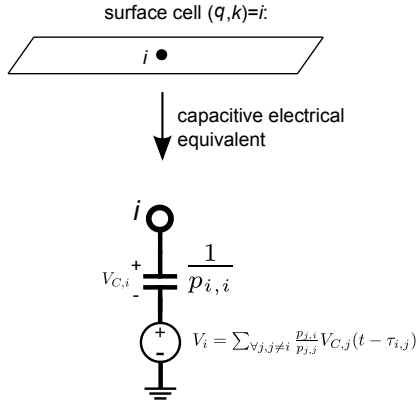


Fig. 4.4: Capacitive PEEC-model for a surface cell around node i.

Therefore, the node potential consists of two parts: a voltage drop across the pseudo-capacitance $1/p_{i,i}$, and a voltage drop due to the capacitive coupling between surface cells i and j. This shows that eq. (4.10) and therefore eq. (4.6), are equivalent with Fig. 4.4.

4.3.4 Complete PEEC-model

If the resistive, inductive and capacitive PEEC-model for a volume cell (γ, m, l), connecting nodes i and j (Figs. 4.2, 4.3 and 4.4) are combined, the complete PEEC-model of Fig. 4.5 is obtained for the case where the incident electric field is zero.

It is called a *full-wave* model if the time delays τ are not zero. If they are zero, the PEEC-model is called *quasi-static*. It is useful to solve electromagnetic problems with partial elements because it allows to think in terms of lumped elements and voltages and currents.

It is also possible to transform the capacitive branches into a Norton-equivalent. This equivalent is shown in Fig. 4.6. It is equivalent to Fig. 4.5.

Proof that the circuits in Figs. 4.5 and 4.6 are equivalent Call in Fig. 4.5 the current in the i^{th} capacitive branch $i_{C,i}$, as in Fig. 4.6. This current is equal to:

$$i_{C,i} = \frac{1}{p_{i,i}} \frac{d}{dt} \left(V_{n,i} - \sum_{\forall k, k \neq i} \frac{p_{k,i}}{p_{k,k}} V_{C,k}(t - \tau_{i,k}) \right) \tag{4.11}$$

with $V_{n,i}$ the voltage at node i. So, we have,

$$i_{C,i} = \frac{1}{p_{i,i}} \frac{dV_{n,i}}{dt} - \sum_{\forall k, k \neq i} \frac{p_{k,i}}{p_{k,k} p_{i,i}} \frac{dV_{C,k}(t - \tau_{i,k})}{dt} \tag{4.12}$$

But,

$$\frac{1}{p_{k,k}} \frac{dV_{C,k}(t - \tau_{i,k})}{dt} = i_{C,k}(t - \tau_{i,k}) \tag{4.13}$$

So,

$$\frac{dV_{C,k}(t - \tau_{i,k})}{dt} = p_{k,k} i_{C,k}(t - \tau_{i,k}) \tag{4.14}$$

Substituting (4.14) into (4.12), leads to:

$$i_{C,i} = \frac{1}{p_{i,i}} \frac{dV_{n,i}}{dt} - \sum_{\forall k, k \neq i} \frac{p_{k,i}}{p_{i,i}} i_{C,k}(t - \tau_{i,k}) \tag{4.15}$$

This proves that the circuits of Figs. 4.5 and 4.6 are equivalent.

4.3.5 Calculating the partial inductances and the short-circuit-capacitances

The freeware software programmes FastHenry [Kamo 30] and FastCap [Nabo 92], developed at the Computational Prototyping Group of Massachusetts Institute of Technology (M.I.T.) by Jacob White, Mattan Kamon and their colleagues, calculate the Lp- and C_s-matrices respectively, under a quasi-static assumption and with use of the multipole expansion technique for speeding up the calculation process. It is chosen in this work to use these freeware programmes instead of developing code to evaluate the integrals ((4.4) and (4.7)). In literature however [Rueh 72][Bren 73][Bren 79][Garr 95][Rueh 95b][Rueh 72][Rueh 73], there exist closed-form expressions for the partial inductances of two rectangular cells with constant rectangular cross-section if the two cells are orthogonal or parallel. Also, there, closed-form expressions are given for the coefficients of potential between two rectangles, if the rectangles are orthogonal or parallel to each other. The incorporation of FastHenry and FastCap in the PEEC-process is a contribution of this work.

4.3.6 Using the partial inductances and short-circuit capacitances

Once the partial inductances, the resistances and the partial capacitances are calculated, they are combined in a circuit which can be solved in the time- or frequency-domain by a circuit simulator. However, as can be seen from

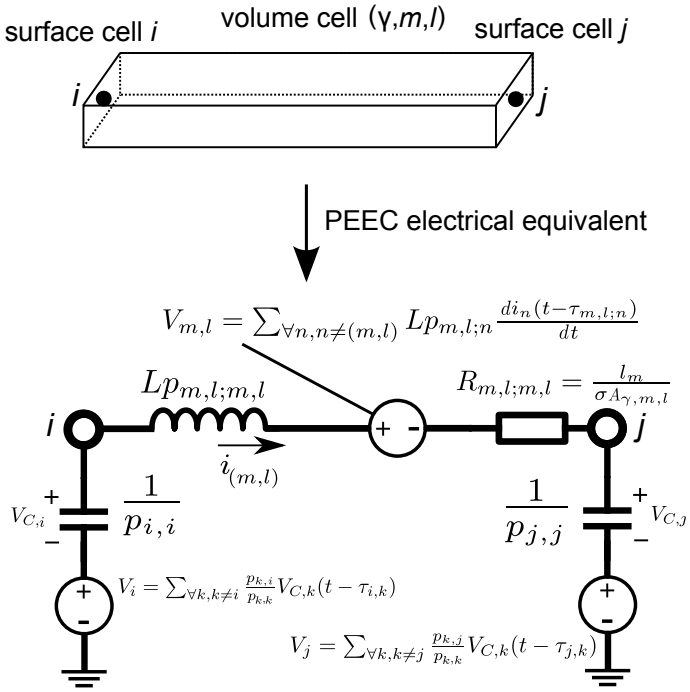


Fig. 4.5: Full PEEC-model for a volume cell (γ, m, l) connecting nodes i and j and its two neighbouring surface cells.

eq. (4.5) and (4.6), the current and charge must be evaluated at the retarded time instances t_n and t_q by this circuit simulator. The flavour of PEEC which takes these retarded times into account is denoted by r-PEEC. The simulator therefore has to solve so-called delay differential equations (DDEs) [Jarl 08]. Solving DDEs is a research topic on its own. In literature [Woll 99], a special Spice solver has been presented in order to cope with retarded times and DDEs. In this work, the standard Spice solver is employed for r-PEEC-calculations, but the LAPLACE-directive is used. Not all Spice-flavours have however such an option. A quasi-static version of PEEC can however still be useful. With the quasi-static PEEC-method, already very high frequencies can be sufficiently accurately taken into account. The highest frequency is determined by the size of the largest geometrical distance in the electrical circuit which must be modelled. This distance must be much shorter than the smallest wavelength present in the signals. As will be showed in next Sections, frequencies of multiple hundreds of megahertz can be accurately modelled with quasi-static PEEC for typical sizes of electrical circuits.

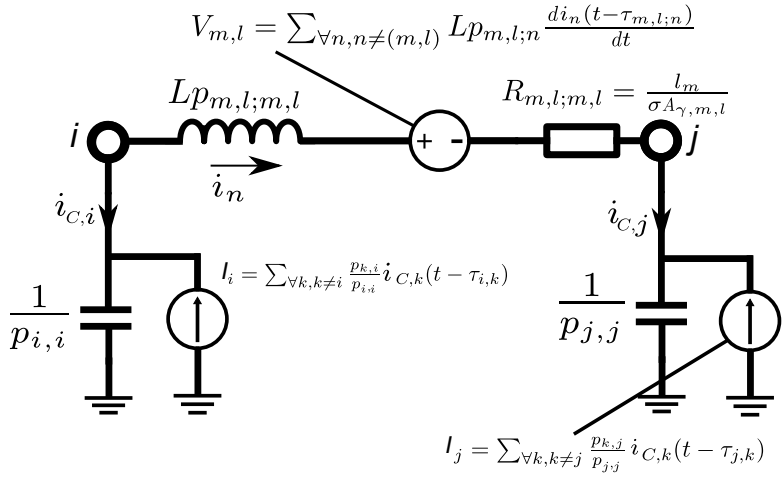


Fig. 4.6: Full PEEC-model for a cell (γ, m, l) connecting nodes i and j, and its two neighbouring surface cells. Norton-equivalent for the capacitive branches.

4.3.7 Modelling the skin-effect

Even though in Section 4.3.2, the current was assumed to be constant over the cross-section, the skin-effect can be modelled well in the PEEC method ([Nits 09], p. 193). An inductive cell is segmented over its cross-section into more elements as shown in Fig. 4.7. Each of these smaller elements has a self-inductance and a resistance. Also, there exist magnetic couplings between these elements. To model the skin-effect in a conductor, the inductive branch of Fig. 4.6 is therefore replaced by a network of parallel RL-branches where magnetic couplings exist between the self-inductances. This is depicted in Fig. 4.8.

Other techniques for modelling the skin-effect are described in Section 4.7 of [Nits 09]. In the PEEC-implementation of this work, it is chosen not to implement the current-redistribution due to the skin-effect. However, FastHenry allows the resistance in the inductive branch of Fig. 4.6 to be dependent on the frequency, so that the total current through the entire branch is determined by its value. As such, the skin-effect is taking into account, albeit not with explicit cross-sectional current redistribution.

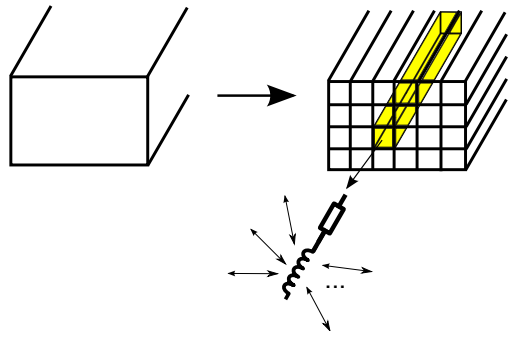


Fig. 4.7: Cross-sectional segmenting of a conductor to account for the skin-effect.

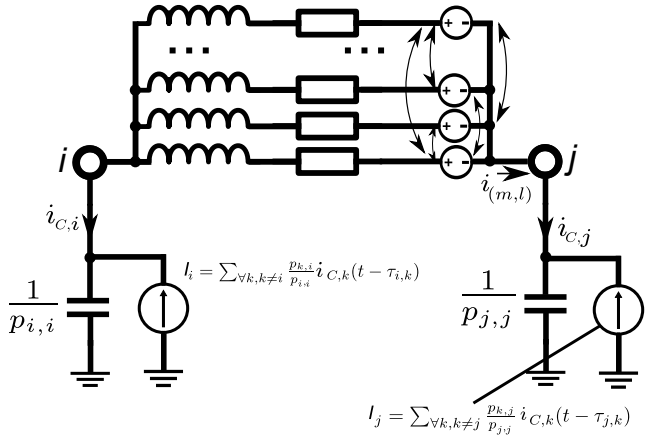


Fig. 4.8: Modelling the skin-effect with the PEEC-method.

4.3.8 Solving the Partial Element Equivalent Circuit

In this Section, it will be shown how the PEEC-circuit of Fig. 4.5 can be solved using Kirchhoff's laws. It will be demonstrated for the frequency-domain case and the time-domain case is very similar. In this work, however, no dedicated solver is developed but instead, PSpice is used. This is a difference from the PEEC-work in literature, where often dedicated solvers are used. The analysis of this Section will prove useful however further on, when the stability of the PEEC-method is addressed.

In order to describe which inductive cells are connected to which nodes in the Partial Element Equivalent Circuit, a connectivity matrix $[A]$ is defined. If there are N capacitive and M inductive cells, $[A]$ is an $M \times N$-matrix, having a

row for each inductive cell and a column for each node. Its elements are mainly zero, and it contains:

- a 1 at position (m, n) if the current in the inductive branch m flows towards node n
- a -1 at position (m, n) if the current in the inductive branch m flows away from node n

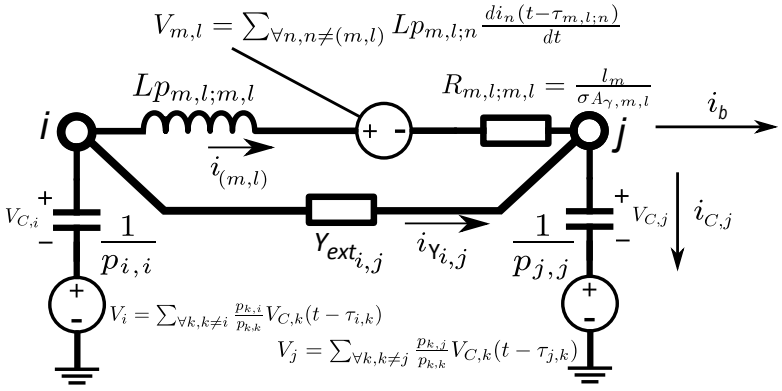


Fig. 4.9: Derivation of the matrix description of the PEEC-model.

Referring to Fig. 4.5, redrawn in Fig. 4.9 with some extra notations and with the addition of external circuit elements $Y_{ext,i,j}$ connected between nodes i and j, the Kirchhoff voltage law can be written for each inductive branch m:

$$\forall\ m = 1, 2, \ldots, M : V_i - sLp_{m,l;m,l} I_{(m,l)} - V_j - \sum_{\forall n, n \neq (m,l)} sLp_{m,l;n} I_n e^{-s\tau_{m,l;n}} - R_{m,l;m,l} I_{(m,l)} = 0 \tag{4.16}$$

If there are also voltage sources in the circuit, the right-hand side is not zero but is this voltage source term (cf. the right-hand side of eq. (4.1)). In matrix form, Kirchhoff's voltage law can be written as:

$$-[A][V] - ([R] + s[L])[I] = [V_s] \tag{4.17}$$

With $[A]$ the connectivity matrix, $[V]$ the vector containing the nodal voltages, $[I]$ the vector containing the inductive branch currents, $[V_s]$ the vector containing the external voltage sources, and $[R]$ and $[L]$ the resistivity and inductance

matrices, including the phase delays:

$$[R] = \begin{bmatrix} R_{1,1} & 0 & \cdots & 0 \\ 0 & R_{2,2} & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & R_{M,M} \end{bmatrix} \tag{4.18}$$

$$[L] = \begin{bmatrix} Lp_{1,1} & Lp_{1,2}e^{-s\tau_{1,2}} & \cdots & Lp_{1,M}e^{-s\tau_{1,M}} \\ Lp_{2,1}e^{-s\tau_{2,1}} & Lp_{2,2} & \cdots & Lp_{2,M}e^{-s\tau_{2,M}} \\ \cdots & \cdots & \cdots & \cdots \\ Lp_{M,1}e^{-s\tau_{M,1}} & Lp_{M,2}e^{-s\tau_{M,2}} & \cdots & Lp_{M,M} \end{bmatrix} \tag{4.19}$$

Next, Kirchhoff's current law can be written for each node j. Suppose that at node j, inductive branches (m,l) and b are connected and that the current i_b in branch b flows away from node j. The current law then states:

$$\forall\ j = 1, 2, \ldots, N: \quad I_{(m,l)} = I_b + I_{Cj} - I_{Y,i,j} = I_b + sC_{j,j}V_{C,j} - Y_{ext,i,j}(V_i - V_j) \tag{4.20}$$

With $C_{j,j} = 1/p_{j,j}$ and $Y_{ext,i,j}$ the admittance of the external lumped component, placed between node i and j. When there are also external current sources, these have to be taken into account as well. In matrix form, previous equation becomes,

$$s[F][V_C] - [A]^T[I] + [Y_{ext}][V] = [I_s] \tag{4.21}$$

$[I_s]$ is the vector of external current sources. $[V_C]$ is the vector containing the voltages across the pseudo-capacitances $1/p_{j,j}$. $[F]$ is an $N \times N$ diagonal matrix, with elements $F_{k,k} = C_{k,k} = 1/p_{k,k}$. $[Y_{ext}]$ is an $N \times N$ admittance matrix, containing for each external admittance $Y_{ext,i,j}$ between node i and j, through which the positive current flows from i to j, an element $+Y_{ext,i,j}$ at the two positions (i,i) and (j,j) and an element $-Y_{ext,i,j}$ at the two positions (i,j) and (j,i). The external voltage and current sources are depicted in Fig. 4.10.

Finally, the nodal potentials equation can be written as, for each node j:

$$\forall j = 1, 2, \ldots, N: \qquad V_j = V_{C,j} + \sum_{\forall k, k \neq j} \frac{p_{j,k}}{p_{k,k}} V_{C,k} e^{-s\tau_{j,k}\prime} \tag{4.22}$$

In matrix form, this becomes:

$$-[V] + [S][V_C] = 0 \tag{4.23}$$

where $[S]$ is an $N \times N$ matrix with elements:

$$S_{i,j} = \frac{p_{i,j}}{p_{j,j}} e^{-s\tau_{i,j}\prime} \tag{4.24}$$

Note that this element reduces to 1 for $i = j$. From this equation, we can find that $[V_C] = [S]^{-1}[V]$. So, the matrix equation of Kirchhoff's current law becomes:

$$s[F][S]^{-1}[V] - [A]^T[I] + [Y_{ext}][V] = [I_s] \tag{4.25}$$

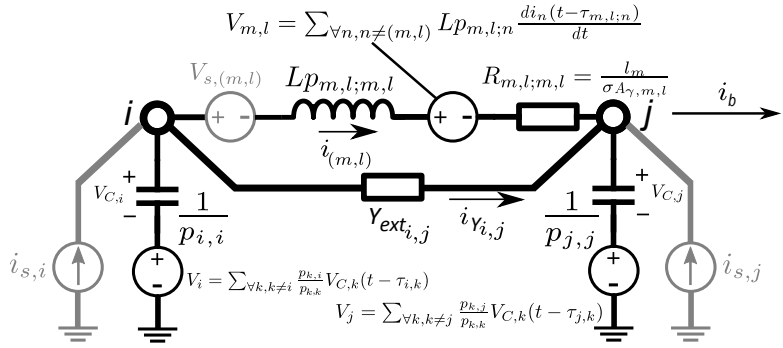


Fig. 4.10: The PEEC-model of a current cell and the two neighbouring voltage cells, together with external sources (in grey) and lumped components.

But, $[S][F]^{-1} = [P]$, with $[P]$ the matrix of the retarded coefficients of potential:

$$[P] = \begin{bmatrix} p_{1,1} & p_{1,2}e^{-s\tau_{1,2'}} & \cdots & p_{1,N}e^{-s\tau_{1,N'}} \\ p_{2,1}e^{-s\tau_{2,1'}} & p_{2,2} & \cdots & p_{2,N}e^{-s\tau_{2,N'}} \\ \cdots & \cdots & \cdots & \cdots \\ p_{N,1}e^{-s\tau_{N,1'}} & p_{N,2}e^{-s\tau_{N,2'}} & \cdots & p_{N,N} \end{bmatrix} \tag{4.26}$$

Note that the delays $\tau_{i,j}$ and $\tau_{i,j'}$ in the matrices $[L]$ and $[P]$ are not the same, because the segmentation in inductive and capacitive cell is different.

Both Kirchhoff laws can now be reformulated into one matrix equation, as follows:

$$\begin{bmatrix} -A & -(R+sL) \\ sP^{-1} + Y_{ext} & -A^T \end{bmatrix} \begin{bmatrix} V \\ I \end{bmatrix} = \begin{bmatrix} V_s \\ I_s \end{bmatrix} \tag{4.27}$$

Or, because $[S][F]^{-1} = [P]$, and $[P]^T = [P]$, we have $[S]^T[P]^{-1} = [F]^3$ and

$$\begin{bmatrix} -A & -(R+sL) \\ sF + S^T Y_{ext} & -S^T A^T \end{bmatrix} \begin{bmatrix} V \\ I \end{bmatrix} = \begin{bmatrix} V_s \\ S^T I_s \end{bmatrix} \tag{4.28}$$

Or,

$$[M(s)] \begin{bmatrix} V \\ I \end{bmatrix} = \begin{bmatrix} V_s \\ S^T I_s \end{bmatrix} \tag{4.29}$$

This is the system matrix equation to solve the nodal voltages and inductive branch currents of the Partial Element Equivalent Circuit in the frequency-domain. It can be easily transformed for time-domain problems, by replacing s by a time derivative operator and $e^{-s\tau_{i,j}}$ by a time delay $t - \tau_{i,j}$. The system matrix description can be found in most of the literature about PEEC.

[3]This is because the operations of transpose and inverse commute for square regular matrices $[X]$: $\left([X]^T\right)^{-1} = \left([X]^{-1}\right)^T$

4.3.9 Stability of the PEEC method

The stability of the PEEC-method is determined by

- The stability of the physical equation governing the system. This is the electric field integral equation (EFIE) and as is the case with most physical laws, it is stable.
- The way the solution domain is discretized.
- The numerical method of solving the discretized equations. For Spice users, the option to choose the numerical integration technique between the backward-Euler method, the trapezoidal method and the Gear method (i.e. a Backward Differentiation Formula (BDF) implicit integration technique, suited for stiff problems) usually eliminates this source of instability.

Let us have a look at the influence on the stability of the way the solution domain is discretized. The discretization of the EFIE leads to a matrix equation (4.28). This is a system of neutral delay differential equations (DDEs) [Jarl 08][Mich 07]. The characteristic roots are those s in the complex plane that satisfy $\det(M(s)) = 0$. They correspond to solutions of the system of DDEs of the type $[x(t)] = e^{st}[x_0]$ for some $[x_0] \in \mathbb{R}^{M+N}$, with $[x]$ the state vector, containing all nodal voltages and branch currents.

A fundamental result for DDEs is that if the characteristic roots are all in the open left-half plane then the set of DDEs is stable (i.e. $[x(t)] \to 0$, for any initial condition of the system, when no input is applied to the system and $t \to \infty$). The more precise formulation of this is given in Proposition 1.22 in [Mich 07]. Equivalently, the condition can be expressed as: $\det(M(s)) \neq 0$, for all s in the right-half plane (plus imaginary axis), i.e., matrix $M(s)$ is invertible for all s in the right-half plane (plus imaginary axis).

In [Rueh 95a], it is shown that a quasi-static PEEC model, i.e. a model where all delays $\tau_{i,j}$ are zero, has characteristic roots on the imaginary axis. It is therefore marginally stable. Another result is that $s = 0$ is always a root for quasi-static or full-wave models. This is an important finding because it is due to this root that the system has a reduced low frequency accuracy. When there are delays in the circuit, the situation changes and the roots of $\det(M(s)) = 0$ have to be calculated. Jarlebring developed an algorithm for this purpose [Jarl 10].

In [Garr 98] and [Rueh 95a], it is stated that the main reason for instability and a bad accuracy is the inaccurate calculation of the delays between the inductive and capacitive cells. In this doctoral work, the delay is assumed constant for each pair of cells, and approximated as the centre-to-centre delay. Reference [Garr 98] suggests a more accurate subdivision of the cells to calculate the

partial inductances and coefficients of potential without increasing the number of unknowns in the circuit. However, it is stated that this technique is intended to improve the accuracy and stability in the *extended* frequency range which corresponds to the range $[f_{max}, 50f_{max}]$, with f_{max} the frequency corresponding to a segmentation in segments of size $c/(20f_{max})$ with c the speed of light. A stabilization scheme is given in [Rueh 95a], where each self-inductor is split in two inductances having mutual magnetic couplings between them. The propagation delay between these two elements is used as a tuning factor to shift the characteristic roots to the open left-half plane. The presence of a mutual inductance causes the net self-inductance to be complex and have a real part, which causes dampening. This idea of dampening to improve stability is further used in [Garr 98]. There, a stabilization scheme is given, which is called an R-ind filter in [Ekma 06]. In parallel with the self-inductances a large resistor is placed to provide dampening at high frequencies. Also, an R-cap filter exists, where a small resistor is placed in series with each pseudo-capacitor $1/p_{ii}$. It can moreover be concluded that a system which consists of only reactive elements and no resistances and which has only perfectly electrically conductive wires, is typically more unstable than a circuit with wires having a finite conductivity.

Example of stability analysis

The stability of one of the simplest circuits shall now be investigated. The method and example of [Rueh 95a] is followed but the fast algorithm of [Jarl 10] is applied. The circuit is a rectangular trace of length 10 cm, width 2 cm and thickness 1 mm and is subdivided into two inductive cells and three capacitive cells (Fig. 4.11). The propagation delays between the capacitive cells are $\tau_{12}\prime = \tau_{21}\prime = \tau_{23}\prime = \tau_{32}\prime = \tau_1\prime$ and $\tau_{13}\prime = \tau_{31}\prime = \tau_2\prime$. The delay between the inductive cells is denoted by τ_L. With these notations, the system matrix $[M(s)]$ for a PEEC-formulation in the frequency domain becomes:

$$\begin{bmatrix} 1 & -1 & 0 & -Rp_{1,1} - sLp_{1,1} & -sLp_{1,2}e^{-s\tau_L} \\ 0 & 1 & -1 & -sLp_{2,1}e^{-s\tau_L} & -Rp_{2,2} - sLp_{2,2} \\ \frac{s}{p_{1,1}} & 0 & 0 & 1 - \frac{p_{2,1}}{p_{1,1}}e^{-s\tau_1\prime} & \frac{p_{2,1}}{p_{1,1}}e^{-s\tau_1\prime} - \frac{p_{3,1}}{p_{1,1}}e^{-s\tau_2\prime} \\ 0 & \frac{s}{p_{2,2}} & 0 & \frac{p_{1,2}}{p_{2,2}}e^{-s\tau_1\prime} - 1 & 1 - \frac{p_{3,2}}{p_{2,2}}e^{-s\tau_1\prime} \\ 0 & 0 & \frac{s}{p_{3,3}} & \frac{p_{1,3}}{p_{3,3}}e^{-s\tau_2\prime} - \frac{p_{2,3}}{p_{3,3}}e^{-s\tau_1\prime} & \frac{p_{2,3}}{p_{3,3}}e^{-s\tau_1\prime} - 1 \end{bmatrix} \quad (4.30)$$

The algorithm of [Jarl 10] is applied to calculate the roots of $\det(M(s)) = 0$. $M(s)$ is rewritten in the form $M(s) = M_A(s) - sM_E(s)$, with $M_A = A_1 + A_2e^{-s\tau_1\prime} + A_3e^{-s\tau_2\prime}$ and $M_E = E_1 + E_2e^{-s\tau_L}$. The algorithm first cannot be applied because $A_1 + A_2 + A_3$ is singular. Therefore, the transformation $s = s' + ss$ is applied. The equation $\det(M(s')) = 0$ is solved in s' and next ss is added to the obtained solutions for s' in order to find s. For a shift $ss = 10^9$, we find the spectrum shown in Fig. 4.12. In order to be sure that the algorithm indeed calculates the roots of $\det(M(s')) = 0$, the minimal singular value of $M(s')$ is calculated for each found root s'. It is shown in Fig. 4.13. They are

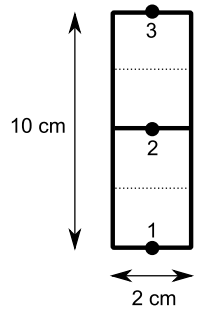


Fig. 4.11: A simple circuit consisting of two inductive cells and three capacitive cells, used in order to study the stability of the PEEC-method.

all smaller than 10^{-8} and therefore it is reasonable that $M(s')$ is singular for the found s'-values. Most of the roots are located in the open left half-plane, but there is one root, 0, on the imaginary axis. There are however no roots in the open right half-plane. Therefore, the system is marginally stable.

It is not easy to automate the procedure to calculate the spectrum for an arbitrary geometry, as due to symmetries in the geometry some time delays can have the same values, and the matrices $M_A(s)$ and $M_E(s)$ will therefore change accordingly.

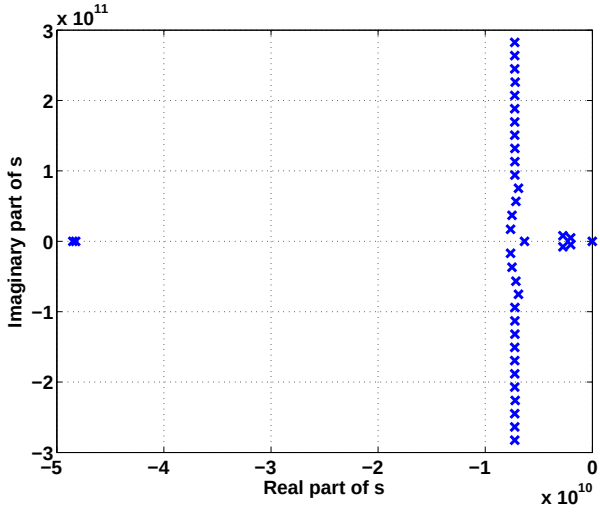


Fig. 4.12: The solutions of $\det(M(s)) = 0$ for the simple circuit of Fig. 4.11.

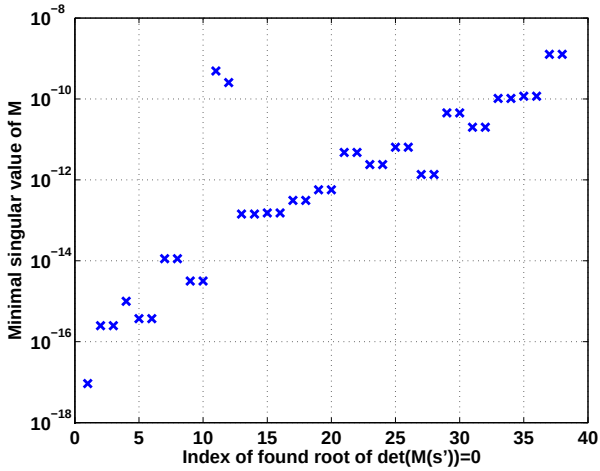


Fig. 4.13: The minimal singular values of M for each found root of the spectrum of Fig. 4.12.

4.4 Method for extraction of an equivalent circuit of a PCB-network

4.4.1 Topology and components of a resistance-divider network

The subsequent steps of the method for modelling the parasitics of a PCB-circuit will now be discussed with an example: a resistance-divider network which is presented in Fig. 4.14. All dimensions are in millimetres, except on the axes where they are expressed in metres. The tracks are 1.2 mm wide and 35 μm thick and are made from copper having a conductivity of $5.8108 \cdot 10^7$ S/m. The point of the track where resistor R_s is attached to, has coordinates (0,0). The copper tracks are printed on a substrate with relative permittivity $\epsilon_r = 4.5$ and with corners (-10, -71), (50.2,-71), (-10, 10), and (50.2, 10) mm, therefore having a width of 60.2 mm and a height of 81 mm. The substrate has a thickness of 1.55 mm.

A voltage source with an output resistance of $R_s = 50\ \Omega$ produces a step voltage V_s. This voltage is applied to the series connection of the resistors $R_{L1} = 51\ \Omega$ and $R_{L2} = 300\ \Omega$. Also, there are some capacitors present in the circuit. They are $C_{L1} = 10$ pF and $C_{L2} = 27$ pF.

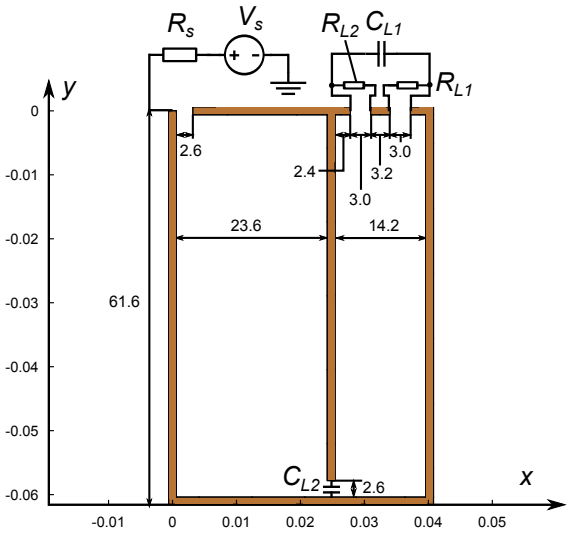


Fig. 4.14: Resistance-divider circuit; the dimensions on the axes are in metres and the others in millimetres.

4.4.2 Using FastHenry to extract the resistances and the inductance matrix

FastHenry calculates the self-resistances and the self- and mutual inductances of the conductors and conductor-pairs. A quasi-static operation is assumed in order to make the calculation process more easy. The structure of the conductors needs to be partitioned in smaller segments through which the current stays constant and on which the charge is uniformly distributed. Each segment needs to be much smaller than the smallest occurring wavelength. If Δl is the length of a segment, and λ_{min} is the smallest wavelength, the rule-of-thumb which is used to determine the length of a segment is:

$$\Delta l < \frac{\lambda_{min}}{10} \tag{4.31}$$

When the size of the structure under consideration becomes large, or when the highest occurring frequency has a high value, time delay effects due to the finite speed of propagation of the electromagnetic waves become important. For segments in the structure that are far apart, the mutual inductances (and mutual capacitances), calculated with the quasi-static assumption, may cause the voltages and currents on different segments to couple with the wrong phase.

The phase error is still tolerable if the size of the structure Δr is such that:

$$\Delta r << \lambda_{min} \tag{4.32}$$

say $\Delta r < \lambda_{min}/10$. Because in the example circuit $\Delta r = \sqrt{61.6^2 + 41.4^2} = 74.2$ mm, and thus $\lambda_{min} = 742$ mm, the highest allowable frequency is $c/\lambda_{min} \approx 400$ MHz, where $c = 299792458$ m/s is the speed of light. Therefore, the length of the segments must be, according to (4.31) smaller than $742/10 = 74.2$ mm. In Fig. 4.15, the input for FastHenry is presented. There are nine segments, numbered with the numbers with the large font size, between 12 nodes, numbered with the numbers with the smaller font size. Also, it can be seen that the segment between nodes 8 and 10 is split in two segments: 6 and 7, because the node 9 must exist in order to connect a capacitor to it. FastHenry calculates the impedance matrix $[R] + j\omega[L]$ for a frequency of 1 MHz, but the quasi-static assumption implies that all inductances are frequency-independent.

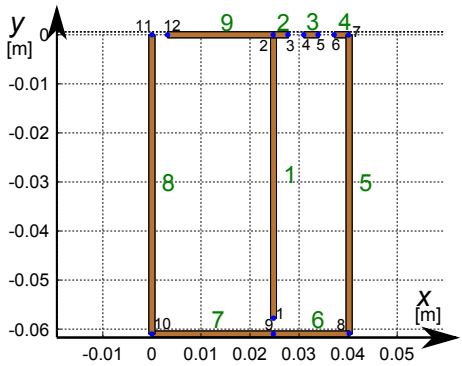


Fig. 4.15: Partitioning the resistance-divider circuit for FastHenry.

Moreover, in order to take the skin-effect into account, the segments can be partitioned further in their width-direction and in their height-direction in smaller filaments. The thickness of the thinnest filament must be smaller than the skin depth δ of the current in the conductor:

$$\delta = \sqrt{\frac{1}{\pi f \sigma \mu}} \tag{4.33}$$

$$\delta > \begin{cases} \dfrac{W}{2\sum_{i=0}^{nwinc/2-1}(rw)^i} & \text{if } nwinc = \text{even;} \\ \dfrac{W}{(rw)^{\frac{nwinc-1}{2}} + 2\sum_{i=0}^{(nwinc-1)/2-1}(rw)^i} & \text{if } nwinc = \text{odd.} \end{cases} \tag{4.34}$$

where σ is the conductivity of the material, μ is the permeability and f is the highest occurring frequency of the current. For 400 MHz, the skin depth is equal

to 3.3 μm. W is the total width of the conductor, rw is the ratio of the widths of two adjacent filaments and $nwinc$ is the total number of filaments in the width-direction (Fig. 4.16). Also call H the height of the conductor, rh the ratio of the heights of two adjacent filaments and $nhinc$ the total number of filaments in the height-direction. A similar equation as (4.34) can be written for the filaments in the height-direction. Because the current in a plane conductor is distributed exponentially, a good approximation for rw or rh is $2 \ldots 3$ ($e \approx 2.718$). Then, $nwinc$ can be determined and added to the input file for FastHenry. For a track width of 1.2 mm, a height of 35 μm and the skin depth at 400 MHz, if $rw = rh = 2.7$, then $nwinc = 12$ and $nhinc = 5$

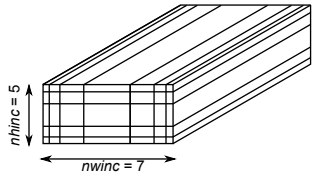


Figure 4.16: Meaning of *nwinc* and *nhinc* in FastHenry [source: [Kamo 30]].

The input file for FastHenry becomes:

```
*
.Units M
.Default z=0 sigma=5.8108e7
N1 x=0.0248 y=-0.0578 z=0
N2 x=0.0248 y=0 z=0
N3 x=0.0278 y=0 z=0
N4 x=0.031 y=0 z=0
N5 x=0.034 y=0 z=0
N6 x=0.0372 y=0 z=0
N7 x=0.0402 y=0 z=0
N8 x=0.0402 y=-0.061 z=0
N9 x=0.0248 y=-0.061 z=0
N10 x=0 y=-0.061 z=0
N11 x=0 y=0 z=0
N12 x=0.0032 y=0 z=0
E1 N1 N2 w=0.0012 h=3.5e-005 nwinc=12 nhinc=5
E2 N2 N3 w=0.0012 h=3.5e-005 nwinc=12 nhinc=5
E3 N4 N5 w=0.0012 h=3.5e-005 nwinc=12 nhinc=5
E4 N6 N7 w=0.0012 h=3.5e-005 nwinc=12 nhinc=5
E5 N8 N7 w=0.0012 h=3.5e-005 nwinc=12 nhinc=5
E6 N9 N8 w=0.0012 h=3.5e-005 nwinc=12 nhinc=5
E7 N10 N9 w=0.0012 h=3.5e-005 nwinc=12 nhinc=5
E8 N10 N11 w=0.0012 h=3.5e-005 nwinc=12 nhinc=5
E9 N12 N2 w=0.0012 h=3.5e-005 nwinc=12 nhinc=5
.external N1 N2
.external N2 N3
.external N4 N5
.external N6 N7
.external N8 N7
.external N9 N8
.external N10 N9
.external N10 N11
.external N12 N2
.freq fmin=400000000 fmax=400000000 ndec=1
.end
```

FastHenry produces the results of Table 4.1 for the self- and mutual partial inductances. A comparison with the values, calculated in [Rueh 74] is also given. Differences might be due to a slightly different geometry. Therefore, also, inductances of segments 2, 3 and 4 are not stated in the table. The reference work [Rueh 74] did not give a value for $Lp69$, because it is very small.

Table 4.1: Partial inductances computed by FastHenry and in [Rueh 74].

inductance	FastHenry [nH]	[Rueh 74] [nH]	inductance	FastHenry [nH]	[Rueh 74] [nH]
Lp11	56.6	57.2	Lp15	15.2	14.7
Lp55	60.4	62.1	Lp18	11.2	10.6
Lp66	11.1	11.6	Lp58	8.1	7.7
Lp77	20.2	21	Lp67	2.6	2.4
Lp88	60.5	59	Lp69	0.52	NA
Lp99	17.0	20	Lp79	0.86	1

4.4.3 Using FastCap to extract the capacitance matrix

The resistance-divider circuit is partitioned in 12 conductors, each of which is located 'around' each of the 12 nodes. As can be seen in Fig. 4.17, conductors 1, 3, 4, 5, 6, 9, 11 and 12 are straight, conductor 2 has a T-shape, conductor 10 has an L-shape, conductor 8 has the shape of a ⌟ and conductor 7 has the shape of a ⌝. In the Figure, different shades of grey are given to different conductors.

The surface of the conductors is segmented in smaller panels, having a size of 1.2 mm, which corresponds to the width of the PCB-tracks. The top plane of the dielectric substrate is triangularly meshed around each of the conductors (Fig. 4.18) and this mesh is a .qui-input file (*substrate.qui*) for the FastCap-listfile. The substrate has an outer relative permittivity of 1 and an inner relative permittivity of 4.5. As can be seen, there are actually 'holes' in the substrate top plane: these holes are the parts of the substrate top plane with which the bottom side of the copper PCB-tracks make contact. A separate .qui-input file exists for the bottom side of each copper PCB-track, making contact with the substrate. In these .qui-files, the outer relative permittivity is 4.5. The other panels of each copper conductor are part of a different .qui-file and have an outer relative permittivity of 1. Plus signs are used in the listfile to state that the bottom plane of a copper track and the other planes are part of the same conductor. As was already mentioned, the top plane of the dielectric substrate is triangularly meshed and the nodes of this mesh are written to *substrate.qui*. The other five planes of the substrate are meshed in rectangles and the coordinates of the corner points of those rectangles are written to the same .qui-file *substrate.qui*. The input listfile is thus:

```
* list file for capacitive partitions
C cond1.qui 1 0 0 0 +
C cond1_bottom.qui 4.5 0 0 0
C cond3.qui 1 0 0 0 +
C cond3_bottom.qui 4.5 0 0 0
C cond4.qui 1 0 0 0 +
C cond4_bottom.qui 4.5 0 0 0
C cond5.qui 1 0 0 0 +
C cond5_bottom.qui 4.5 0 0 0
C cond6.qui 1 0 0 0 +
C cond6_bottom.qui 4.5 0 0 0
C cond9.qui 1 0 0 0 +
C cond9_bottom.qui 4.5 0 0 0
C cond11.qui 1 0 0 0 +
C cond11_bottom.qui 4.5 0 0 0
C cond12.qui 1 0 0 0 +
C cond12_bottom.qui 4.5 0 0 0
C cond2.qui 1 0 0 0 +
C cond2_bottom.qui 4.5 0 0 0
C cond7.qui 1 0 0 0 +
C cond7_bottom.qui 4.5 0 0 0
C cond8.qui 1 0 0 0 +
C cond8_bottom.qui 4.5 0 0 0
C cond10.qui 1 0 0 0 +
C cond10_bottom.qui 4.5 0 0 0
D substrate.qui 1 4.5 0 0 0 0.0201 -0.0305 -0.0007925 -
```

The minus sign at the end of the last line states that the previous three coordinates, in this case (0.0201,-0.0305,-0.0007925) m, specify a point *inside* the substrate, to distinguish between the inner and outer region.

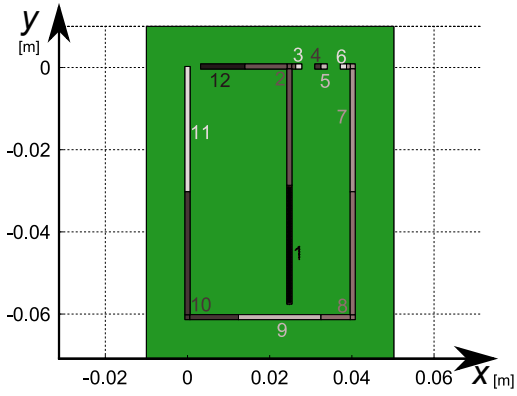


Fig. 4.17: Partitioning the resistance-divider circuit for FastCap.

In fact, FastCap does not produce the regular capacitance matrix Cp, but produces a short-circuit capacitance matrix C_s ([Nabo 92], p. 22). The following transformations exist between the two matrices [Shen 09]:

$$\begin{array}{lcll} Cp_{ii} & = & \sum_{j=1}^{N} C_{sij} & \text{for } i = 1, 2, \ldots, N \\ Cp_{ij} & = & -C_{sij} & \text{for } i \neq j \end{array} \tag{4.35}$$

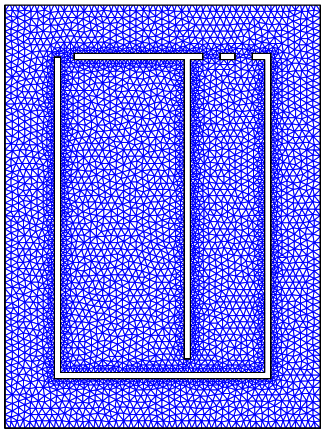


Fig. 4.18: Triangular mesh of the top plane of the dielectric substrate of the resistance-divider circuit: notice the 'holes'.

FastCap produces the results of Table 4.2 for the self and mutual partial capacitances. A comparison with the values of [Rueh 74] cannot be made because in that work the dielectric substrate was not taken into account. Also a comparison with the reported values in other works cannot be made, because either a different segmentation is used or the substrate is not taken into account. Only the capacitances larger than 14 fF are reported in this Table.

Table 4.2: Partial capacitances computed by FastCap.

capacitance	[fF]	capacitance	[fF]	capacitance	[fF]	capacitance	[fF]
Cp(1,1)	616.8	Cp(1,9)	190.4	Cp(4,2)	33.1	Cp(11,12)	133.8
Cp(2,2)	899.2	Cp(1,11)	61.7	Cp(4,7)	21.1	Cp(11,2)	143.9
Cp(3,3)	44.2	Cp(1,12)	14. 7	Cp(5,2)	25.3	Cp(11,7)	52.5
Cp(4,4)	52.0	Cp(1,2)	212.6	Cp(5,7)	28,0	Cp(11,8)	44.2
Cp(5,5)	53.1	Cp(1,7)	82.6	Cp(6,2)	15.9	Cp(11,10)	246.7
Cp(6,6)	52.0	Cp(1,8)	216.7	Cp(6,7)	110.4	Cp(12,2)	189.8
Cp(7,7)	840.1	Cp(1,10)	143.3	Cp(9,11)	24.6	Cp(12,7)	24.9
Cp(8,8)	984.9	Cp(2,7)	222.5	Cp(9,2)	27.8	Cp(7,8)	227.6
Cp(9,9)	499.1	Cp(2,8)	90.5	Cp(9,7)	24.4	Cp(7,10)	50.3
Cp(10,10)	1160.8	Cp(3,2)	120.4	Cp(9,8)	218.1	Cp(8,10)	91.7
Cp(11,11)	848.3	Cp(4,5)	72.5	Cp(9,10)	225.3	Cp(10,12)	23.0

4.4.4 Using Spice to simulate the voltage and current waveforms

The self- and mutual partial inductances, the self-resistances (mutual resistances are not used in this work) and the self- and mutual partial capacitances are

inserted in a Spice subcircuit (.SUBCKT) modelling the PCB-tracks, with respectively the Spice elements L, K, R, C and C. The element K, the coupling coefficient between two inductances, is defined as [PSpi 00]:

$$K_{ij} = \frac{L_{ij}}{\sqrt{L_{ii}L_{jj}}} \tag{4.36}$$

If there are M self-inductances, there are $M(M-1)/2$ mutual inductances. In order to reduce this number and speed up the Spice calculation process, the 20% smallest mutual inductances can be ignored. Also, the 20% smallest mutual capacitances can be neglected.

PSpice by Cadence [Cade] is used as Spice simulation tool. The subcircuit modelling the PCB-tracks, is imported and the external resistors R_{L1} and R_{L2} and capacitors C_{L1} and C_{L2} are connected, together with the voltage source and its 50 Ω-input resistor (Fig. 4.19). Because the simulation results are compared with measurements, not an ideal step voltage is applied, but the applied step voltage was measured and the `VPWL_FILE` element is used in Spice. With this element, a piecewise linear voltage can be specified in a file. The applied step voltage is measured with an oscilloscope and the measured voltage is applied in PSpice with the `VPWL_FILE` element. This voltage is not perfectly a step; it is shown in Fig. 4.20. The voltage across the 51 Ω-resistor is then calculated in function of the time with Spice and is also measured.

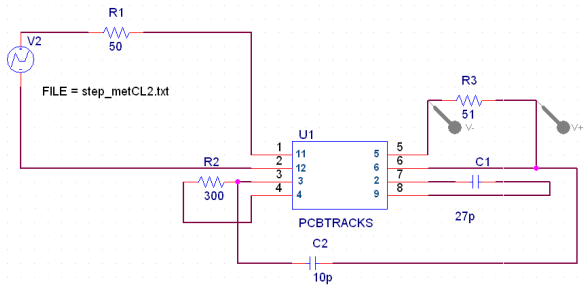


Figure 4.19: Importing the model for the PCB-tracks of the resistance-divider circuit into Spice.

Note that there appears to be no ground node, 0, present in the Spice circuit, when looking at Fig. 4.19. **This is not true!** Inside the subcircuit PCBTRACKS, the partial self-capacitances Cp_{ii} are connected between a node and the ground node 0 in the quasi-static approximation. The ground node 0 thus represents in this work the space at infinity, far away from the circuit, where the stray electric field lines end, thus causing the existence of a partial self-capacitance. Also, in order to improve convergence, a high-impedance resistor of 100 MΩ is connected in parallel with each partial self-capacitance.

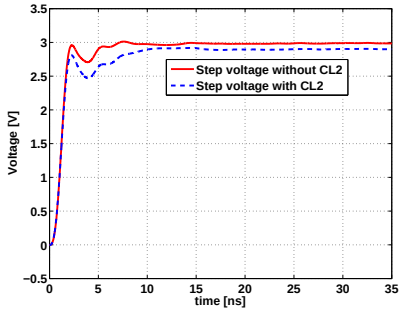
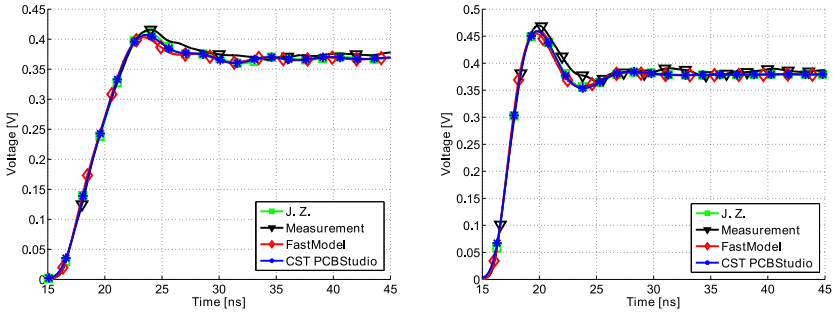


Figure 4.20: Input step voltages of the resistance-divider circuit.

4.4.5 Results

The Spice simulation results are compared with measurements, with the results of a commercial partial element equivalent circuit simulator (CST PCB Studio [CST]) and with the results of a Method of Moments based circuit simulator which does not take the dielectric substrate into account and is developed by J. Zwysen from KU Leuven [Zwys 12]. Also in the simulator of J. Zwysen and in CST PCB Studio, the input voltage is equal to the measured step voltage. Two cases are considered: the circuit with the capacitor C_{L2} and the circuit without this capacitor. For each case, the input step voltage is slightly different. The results are shown in Fig. 4.21. As can be seen, the measurement data agree very well with the behaviour predicted by the method of this work, and also with the results produced by CST PCB Studio and the Moment Method technique of [Zwys 12]. In fact, these last two results are almost identical. The method of this Chapter, making use of FastHenry, FastCap and Spice, produces results that predict very well the rise times, overshoots, oscillation behaviours and steady state values of the voltage across the 51 Ω-resistor. The most important conclusion that can be drawn from these simulations and measurements, is that the exact layout of the PCB-tracks is of great importance for the behaviour of the voltages and currents when fast changing (step) voltage excitations occur. As a comparison, the voltage across R_{L1} is shown in Fig. 4.22 when in Spice ideal connections are used between the circuit elements. Comparison of Figs. 4.21 and 4.22 learns that the parasitics of the copper PCB-tracks indeed have significant influence on the electrical signals.



(a) Voltage across R_{L1} with $C_{L2} = 27$ pF. (b) Voltage across R_{L1} with $C_{L2} = 0$ pF.

Figure 4.21: Voltage across R_{L1}, with and without C_{L2}.

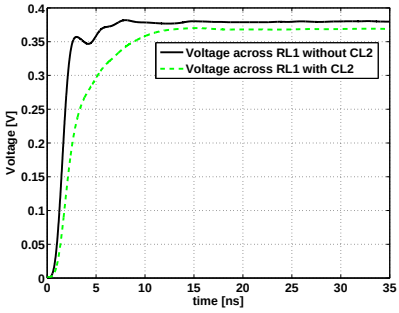


Figure 4.22: Voltage across R_{L1} for ideal connections.

4.4.6 Extending the PEEC-method to full-wave capability

In order to model PCB-tracks at very high frequencies, at which the wavelength becomes comparable to the circuit dimensions, a quasi-static technique is no longer sufficient but a full-wave technique is needed. In order to develop this, the partial self-resistances $R_{m,l;m,l}$ and self-inductances $Lp_{m,l;m,l}$ of Fig. 4.5 are extracted with FastHenry and the pseudo-capacitances $1/p_{i,i}$ are determined by calculating the short-circuit capacitance matrix $[C_s] = [P]^{-1}$ with FastCap. Then, in order to complete the model of Fig. 4.5, the mutual inductive interactions are modelled with a series connection $V_{m,l}$ of voltage sources and the mutual capacitive interactions are modelled with a series connection V_i of voltage sources. $V_{m,l}$ and V_i employ *delayed* voltages. Spice therefore has to solve delay-differential equations (DDEs) [Jarl 08]. In the PSpice-file, these delayed sources are modelled as E-elements (voltage-controlled voltage sources), with the LAPLACE option. This is an entirely new contribution of this work. If the delayed source which is present between nodes Nx (=positive node) and

Ny (=negative node), can be written as:

$$Lp\frac{di(t-\tau)}{dt} \tag{4.37}$$

it is modelled as an E-element as follows:

```
E_Lp Nx Ny LAPLACE {V(INPOS, INNEG)}={s*exp(-s*tau)*Lp}
```

This is true because taking a derivative in the time-domain corresponds with a multiplication with the Laplace variable s in the Laplace domain and because a time-delay with time τ corresponds with a multiplication with $e^{-\tau s}$ in the Laplace domain. According to eq. (4.37), $V(INPOS, INNEG)$ should be the Laplace transform of the *current* $i(t)$. However, because only the voltage-controlled sources can deal with the LAPLACE-directive, $i(t)$ has to be transformed to a voltage with the same value, therefore equal to the voltage when the current flows through a resistance of 1 Ω. This current-to-voltage transformation is accomplished in Spice with a current-controlled voltage source H.

Instead of implementing the mutual couplings in the inductive branch of Fig. 4.5 with a derivative of a current source, also a voltage source implementation can be used. This increases the numerical stability of the implementation. This can be easily done as follows. The mutual inductive coupling between current element m and current element n is:

$$Lp_{m,n}\frac{di_n(t-\tau_{m,n})}{dt} \tag{4.38}$$

This is the same as:

$$\frac{Lp_{m,n}}{Lp_{n,n}}Lp_{n,n}\frac{di_n(t-\tau_{m,n})}{dt} = \frac{Lp_{m,n}}{Lp_{n,n}}V_{L,n}(t-\tau_{m,n}) \tag{4.39}$$

with $V_{L,n}$ the voltage across the partial self-inductor $Lp_{n,n}$. It is this method that is used in the PEEC-implementation of this work, the software code PCBParC (see Section 4.9).

Analogously, also the mutual capacitive couplings can be implemented with a LAPLACE-directive in Spice. If the delayed source of Fig. 4.5 is present between nodes Nx (=positive node) and Ny (=negative node) and can be written as:

$$pV(t-\tau) \tag{4.40}$$

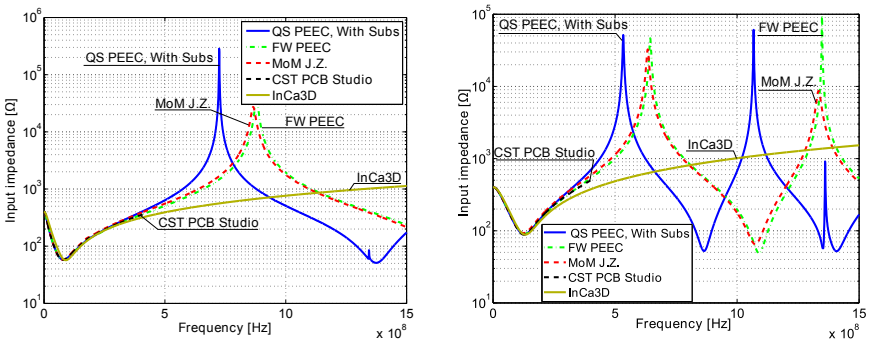
it is modelled as an E-element as follows:

```
E_Cp Nx Ny LAPLACE {V(INPOS, INNEG)}={exp(-s*tau)*p}
```

Not all flavours of Spice can deal with the LAPLACE-directive; however, PSpice and LTSpice can. HSpice and T-Spice are able to work with the LAPLACE-option, but only for rational transfer functions. Ngspice and Spice Opus can indirectly handle a frequency response. They do not have a LAPLACE-directive, but can work with XSPICE code model equivalents for the s-domain description, such as `x_fer`, which can handle rational transfer functions.

4.4.7 Input impedance of the resistance-divider circuit

The magnitude of the input impedance of the resistance-divider circuit is determined, in the frequency-range from 100 kHz till 1.5 GHz. Referring to Fig. 4.14, voltage source V_s is now a sinusoidal source. The input current is determined and the ratio of input voltage and input current gives the input impedance. The results are shown, for the cases where C_{L2} is present or not, respectively in Figs. 4.23a and 4.23b. The results of the full-wave PEEC-method and the Method of Moments, implemented by Jeroen Zwysen [Zwys 12], agree very well. Neither of the implementations of these methods allow the dielectric substrate to be modelled, so in order to see what happens when the substrate is present, the quasi-static PEEC-method is used. It can be seen that the presence of the substrate makes the resonances occur at lower frequencies. Of course, care has to be taken regarding the validity of the quasi-static PEEC-results. They are only valid up to 400 MHz, as explained in Section 4.4.2. Also, a comparison with commercial software programmes, PCB Studio by CST [CST], and InCa3D by Cedrat [Cedr], is given. Both of these programmes implement a quasi-static PEEC-method; in fact PCB Studio only allows the simulation to have as maximum frequency 413 MHz, whereas InCa3D simulates the entire frequency range without giving a warning that the results are not reliable above a specific frequency. PCB Studio allows to model dielectrics, InCa3D does not.



(a) C_{L2} present.

(b) C_{L2} not present.

Figure 4.23: Simulated input impedance of the resistance-divider circuit.

4.4.8 Testing the validity of the capacitance extraction method

The method of extracting the short-circuit capacitance matrix with FastCap is explained in Section 4.4.3. The interfaces between the metallic conductors and the dielectric substrate are omitted from the top plane of the substrate. These interfaces are part of the metallic conductors however, and are present in a surrounding medium having a relative permittivity equal to the relative permittivity of the substrate. The other boundary planes of the metallic conductors are present in a surrounding medium with a relative permittivity of 1. In order to validate this idea, two test cases are set up:

- The capacitance of a parallel plate capacitor
- The capacitance per unit length between two strips printed on the same side of a substrate

Capacitance of a parallel plate capacitor

The geometry of a parallel plate capacitor is depicted in Fig. 4.24. It has two metal plates of 5 cm x 5 cm, having a thickness of 1 mm. The plates are 3 mm apart and there is a 3 mm thick dielectric between the plates having a relative permittivity of 10. The theoretical capacitance is:

$$C_{theor} = \frac{\epsilon_r \epsilon_0 A}{d} = \frac{10 \cdot 8.85 \cdot 10^{-12} \cdot 25 \cdot 10^{-4}}{0.003} = 7.375 \cdot 10^{-11}\ F$$

This was simulated in FastCap with following lst-file:

```
* list file for capacitive partitions
C cond1_simplecap.qui 1 0 0 0 +
C cond1_simplecap_bottom.qui 10 0 0 0
C cond2_simplecap.qui 1 0 0 0 +
C cond2_simplecap_top.qui 10 0 0 0
D substrate_simplecap.qui 1 10 0 0 0 0 0 0
```

This lst-file states that the capacitor has two metallic plates, *cond1* and *cond2*, representing the top and the bottom plates respectively. The bottom face of the top plate, denoted by *cond1_simplecap_bottom* has a surrounding relative permittivity of 10, while the other 5 faces of the top plate, denoted by *cond1_simplecap*, are present in air with a relative permittivity of 1. The top face of the bottom plate, denoted by *cond2_simplecap_top* has a surrounding relative permittivity of 10, while the other 5 faces of the bottom plate, denoted by *cond2_simplecap*, are present in air with a relative permittivity of 1. The substrate has an outer relative permittivity of 1 and an inner of 10, and lacks a

top and a bottom face: it only consists of its 4 side faces. When the size of the panels is 1 mm×1 mm, the capacitance calculated by FastCap, is 76.48 pF, and hence the error is small, only (7.648-7.375)/7.375 = 3.7 %.

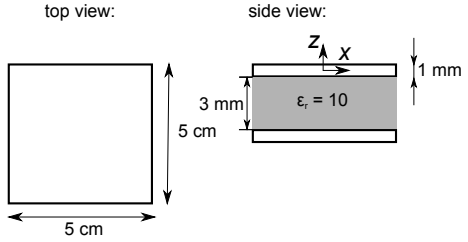


Figure 4.24: Geometry of the parallel plate capacitor test case.

Capacitance per unit length between two strips printed on the same side of a substrate

Two copper tracks of 5 mm high, 10 mm wide and 10 cm long, are present on a substrate with thickness 3 cm and relative permittivity 40. They are separated 1 cm from each other and 1 cm from the edge of the substrate, as shown in Fig. 4.25. They are segmented in panels for FastCap with a size of 5 mm×5 mm.

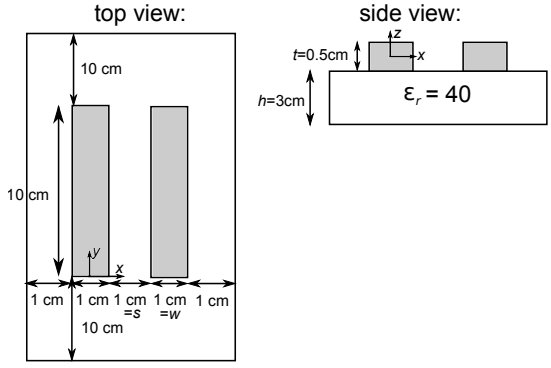


Figure 4.25: Geometry of the two tracks on substrate test case.

Clayton R. Paul's book [Paul 06] gives following theoretical expressions for the characteristic impedance on p. 202-203:

$$Z_c = \begin{cases} \frac{120}{\sqrt{\epsilon'_r}\ln\left(2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right)} & \text{if } \frac{1}{\sqrt{2}} \leq k \leq 1; \\ \frac{377\pi}{\sqrt{\epsilon'_r}\ln\left(2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right)} & \text{if } 0 \leq k \leq \frac{1}{\sqrt{2}}. \end{cases} \tag{4.41}$$

where k is

$$k = \frac{s}{s + 2w} \tag{4.42}$$

and $k' = \sqrt{1 - k^2}$. The effective relative permittivity is

$$\begin{aligned} \epsilon'_r &= \frac{\epsilon_r + 1}{2} \tanh\left(0.775 \ln\left(\frac{h}{w}\right) + 1.75\right) \\ &\quad + \frac{\epsilon_r + 1}{2} \frac{kw}{h} (0.04 - 0.7k + 0.01(1 - 0.1\epsilon_r)(0.25 + k)) \end{aligned} \tag{4.43}$$

This gives us, for $w = 0.01$ m, $t = 0.005$ m, $s = 0.01$ m, $h = 0.03$ m, $\epsilon_r = 40$, a characteristic impedance of $Z_c = 54.199\ \Omega$. The capacitance per unit length is then:

$$C = \frac{1}{vZ_c} \tag{4.44}$$

where the phase speed $v = c/\sqrt{\epsilon'_r}$ and c is the speed of light. For this case, $C = 2.7383 \cdot 10^{-10}$ F/m.

The freeware 2D finite-element programme FEMM [FEMM] is used to check this formula and the results it produced. The electric field is shown in Fig. 4.26. The simulation occurs for a depth of 1 cm. The voltage on the left track is 1 V, the voltage on the right track is -1 V . The charge on the left wire is $5.44532 \cdot 10^{-12}$ C, and is $-5.445 \cdot 10^{-12}$ C on the right track. Therefore, the capacitance per cm is:

$$C_{FEMM} = \frac{5.445 \cdot 10^{-12}}{2} = 2.7225 \cdot 10^{-12}\ F/cm \tag{4.45}$$

corresponding well with the value predicted by eqs. (4.41)-(4.44).

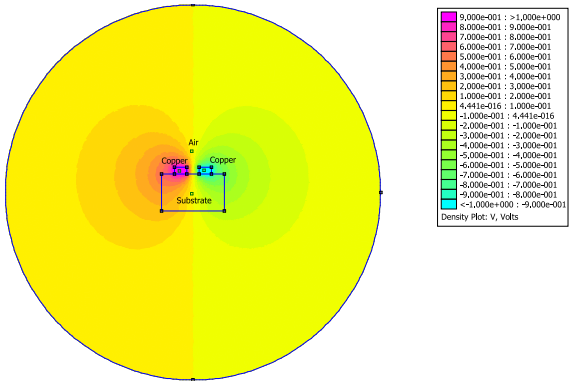


Figure 4.26: FEMM simulation of the two tracks geometry - electric field.

This is also modelled with FastHenry and FastCap. Each conductor is segmented in 10 inductive segments along its length and 11 capacitive segments. For the sake of completeness, the .lst-file for the capacitive segmentations is shown:

```
* list file for capacitive partitions
C cond1.qui 1 0 0 0 +
C cond1_bottom.qui 40 0 0 0
C cond2.qui 1 0 0 0 +
C cond2_bottom.qui 40 0 0 0
...
C cond22.qui 1 0 0 0 +
C cond22_bottom.qui 40 0 0 0
D substrate.qui 1 40 0 0 0 0.01 0.05 -0.0175 -
```

Again, stating that the bottom face of each metallic segment, denoted by *condi_bottom* has a surrounding relative permittivity of 40, while the other 3 or 4 faces of the segment, denoted by *condi*, are present in air, with a relative permittivity of 1. Here, i is a natural number from 1 to 22. The substrate, denoted by *substrate*, has an outer relative permittivity of 1 and an inner of 40. The substrate consists of 4 side faces, 1 bottom face, and 1 top face but this top face has 2 rectangular holes in it, corresponding to the interfaces with the two metallic conductors. x=0.01 m, y=0.05 m, z=-0.0175 m is the centre of gravity of the substrate and the minus sign at the end of the D-statement implicates that the point defined by the three preceding coordinates lies on the inside of the dielectric.

A voltage source of amplitude 1 and frequency 1000 Hz is applied in Spice between two ends of the tracks (Fig. 4.27). A current flows with magnitude 173.74 nA. The theoretical capacitance is $2.7383 \cdot 10^{-12}$ F/m, hence a current of $|j\omega C| = 2\pi \cdot 1000 \cdot 2.7383 \cdot 10^{-10} \cdot 0.1 = 172.1$ nA flows theoretically. The relative error between these two currents is $(173.74 - 172.1)/172.1 = 0.95\%$, indicating that the capacitance extraction method of this work gives sufficiently accurate results.

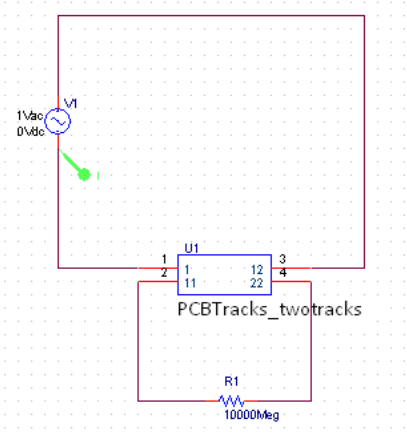


Figure 4.27: Spice simulation of the PEEC model of the two tracks topology.

4.5 Determining the behaviour of a fast switched-mode power supply

4.5.1 Geometry

The method of this Chapter can also be used to determine the currents and voltages of a switched-mode power supply (SMPS). As an example, a so-called reversed buck converter is used. It has almost the same operating principle as an ordinary buck, or step-down, converter, but in the reversed buck topology, the source of the switching transistor is connected with the ground line, thus facilitating the design of the gate-driver, which does not have to be isolated as explained in [Jacq 10]. The topology is depicted in Fig. 4.28 and 4.29 with the dimensions expressed in millimetres (except for the x- and y-axes, being measured in metres). All tracks have a width of 2 mm and a thickness of 35 μm. Point (0,0) is the point in the middle of the lower left corner of the switching cell, and is located at the point $N1$. The switching cell is the region between the input capacitor C_{s2}, the diode D_1 and the switch M_1. As can be seen, the switching cell has a size of more or less 10x10 cm^2. The copper PCB-tracks are printed on a substrate with a relative permittivity of 4.0 and a thickness of 1.55 mm. The substrate has as corner nodes (-56.99,108.77), (235.5,108.77), (-56.99,-59.48) and (235.5,-59.48) mm, therefore having a width of 292.49 mm and a height of 168.25 mm. Table 4.3 shows the components used for the converter. A DC voltage source of 40 V feeds the circuit. The load is a resistor of 15 Ω. The switch is operated at 1 MHz and has a duty cycle of 50 %. Therefore, the output voltage is 20 V and the output current is 1.333 A. Table 4.4 lists the coordinates of the node points.

Table 4.3: Components used in the reversed buck converter.

Component	Type/Value
V_s	40 V, Delta Elektronika SM120-13 adjustable power supply
C_{s1}	2200 μF, 63V, Panasonic ECOS1JP222BA
C_{s2}	220 nF, 63 V, Vishay Roederstein MKT1820422065, 3 caps in parallel
D_1	600 V, 4 A, SiC Schottky diode, Cree C3D04060A
M_1	200 V, 12 A, GaN HFET, EPC-Corp EPC1010
$R_1 = R_2$	0.3 Ω
R_3	0.6 Ω
C_L	100 μF, 100 V, Vishay BC Components MAL213669101E3
R_L	15 Ω, Welwyn WH5010RJI (10 Ω) + Vishay Dale RH0505R000FE02 (5 Ω)
L_1, L_2, L_3	40 μH, 2 A, Epcos B82111EC23

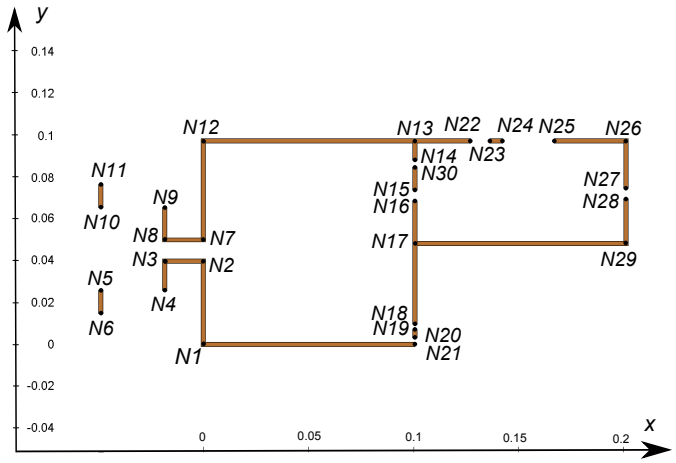


Fig. 4.28: Geometry and dimensions of the reversed buck; the dimensions on the axes are in metre.

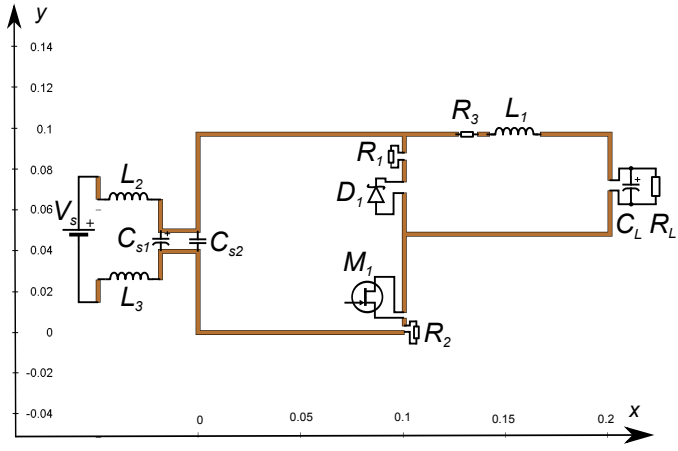


Fig. 4.29: Geometry and components of the reversed buck.

Table 4.4: Node coordinates of the reversed buck converter.

Node	x, y coord. [mm]	Node	x, y coord. [mm]	Node	x, y coord. [mm]
$N1$	0, 0	$N11$	-48.9, 76.1	$N21$	100.6, 0
$N2$	0, 39.55	$N12$	0, 96.7	$N22$	126.97, 96.7
$N3$	-18.4, 39.55	$N13$	100.6, 96.7	$N23$	130.44, 96.7
$N4$	-18.4, 25.55	$N14$	100.6, 87.5	$N24$	136.38, 96.7
$N5$	-48.9, 25.55	$N15$	100.6, 73.46	$N25$	166.87, 96.7
$N6$	-48.9, 14.73	$N16$	100.6, 68.2	$N26$	201.1, 96.7
$N7$	0, 49.7	$N17$	100.6, 48	$N27$	201.1, 74.1
$N8$	-18.4, 49.7	$N18$	100.6, 9.56	$N28$	201.1, 69.1
$N9$	-18.4, 65.03	$N19$	100.6, 7.06	$N29$	201.1, 48
$N10$	-48.9, 65.03	$N20$	100.6, 3.13	$N30$	100.6, 84.2

4.5.2 Using FastHenry to extract the resistances and the inductance matrix

The largest distance between two parts of the reversed buck circuit is 265 mm. Therefore, according to eq. (4.32), $\lambda_{min} = 2650$ mm and the highest allowable frequency is $c/\lambda_{min} \approx 113$ MHz, where $c = 299792458$ m/s is the speed of light. Therefore, the length of the segments must be smaller than $2650/10 = 265$ mm according to eq. (4.31). However, here, we shall arbitrarily use segments with a maximum length of 10 mm. The geometry is then segmented in 79 inductive subdivisions and has 88 nodes. The frequency for which the skin-effect is taken into account, is 1 MHz because this is the most important component in the frequency spectrum of the currents, although other, higher frequencies will also be present. For this frequency, $nwinc = 7$ and $nhinc = 2$.

4.5.3 Using FastCap to extract the capacitance matrix

88 capacitive subsegments (called 'conductors' in FastCap) are used. The surface of the conductors is segmented in smaller panels, having a size of 2 mm, which corresponds to the width of the PCB-tracks. The top plane of the dielectric substrate is triangularly meshed around each of the conductors. Again, an .lst-file is created and FastCap calculates the short-circuit capacitance matrix which can be transformed to the partial self- and mutual-capacitances with formulas (4.35).

4.5.4 Using Spice to simulate the voltage and current waveforms

The self- and mutual partial inductances, the self-resistances (mutual resistances are not used in this work), and the self- and mutual partial capacitances are inserted in a Spice subcircuit (.SUBCKT) modelling the PCB-tracks, with respectively the Spice elements L, K, R, C and C. PSpice is used as Spice simulation tool. The subcircuit modelling the PCB-tracks, is imported and the external resistors, capacitors, coils, diode and transistor are connected, together with the input voltage source (Fig. 4.30). The spice models for the SiC diode and the GaN transistor are downloaded from the website of their manufacturers, Cree and EPC Corporation. From Fig. 4.30, it can be seen how the capacitors, resistors and coils are modelled with their non-ideal components, for instance the equivalent series resistance (ESR). In a first step, the Spice element `VPWL_FILE` was used to import the measured gate-to-source signal and do the simulations with this signal. However, this led to convergence problems, and therefore, an equivalent PULSE source (V5 in Fig. 4.30) was used, having the same rise and fall times (20.853 ns and 19.547 ns), pulse width (0.47585 μs), period (1.000 μs) and voltage levels (0 and 5 V) as the real gate-to-source signal. Also notice the gate resistor (R6=2.375 Ω), the presence of a protecting Zener diode (U10: BZT52C6V2S), and the input capacitance of two measurement oscilloscope probes ($C4 = 13.151$ pF and $C10 = 1$ pF) in Fig. 4.30.

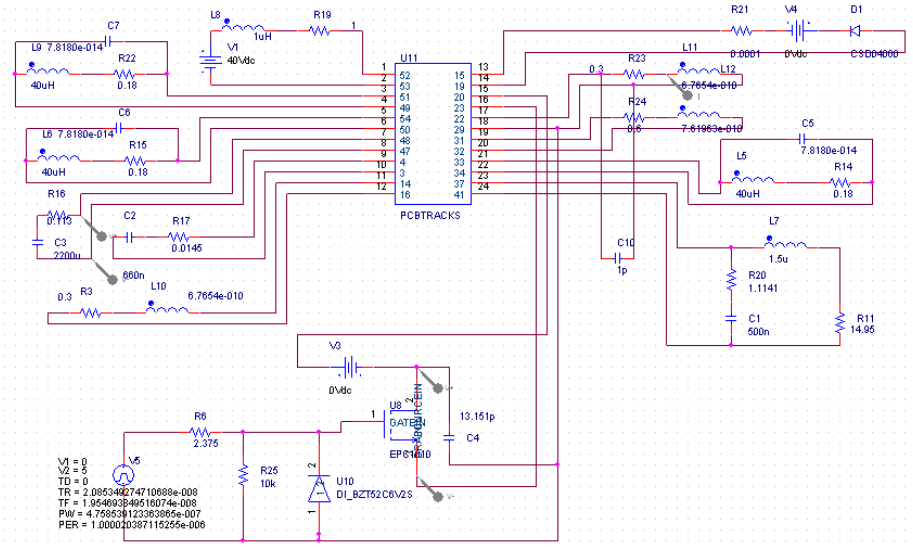


Figure 4.30: Importing the model for the PCB-tracks of the reversed buck circuit into Spice.

4.5.5 Results

All measurements are done with a 500 MHz, 5 GSa/s Tektronix TDS5054 oscilloscope, with 500 MHz Tektronix P5050 voltage probes and the current is measured with the 500 MHz differential probe P6250 from Tektronix, measuring the voltage across the shunts R_1, R_2 and R_3 of Fig. 4.29. The P5050-probe capacitance of about 13.15 pF is taken into account in the simulations, and so is the skin-effect. The simulations and measurements of the voltage across the switch M_1 and the current through the switch M_1 are depicted in Figs. 4.31a and 4.31b respectively.

The measurement and simulation of the voltage show a great resemblance, having almost equal rise, fall times and overshoot. However, the ringing is dampened more in the real situation than in the simulations. The frequency content of the ringing phenomenon corresponds very well. The measurements show a frequency of 14.3 MHz, whereas the simulations predict a frequency of 14 MHz. Furthermore, in the off-state, the simulations show practically no ringing, contradicting the measurements, where a, albeit small, higher frequency ripple is present.

The measurement and simulation of the current also show a good resemblance, especially during the off-time of the switch. The mismatch in the frequency content of the ringing phenomenon is in all cases negligible. The measurements show a frequency of 14 MHz during the off-time of the switch and 38 MHz during the on-time (also there is a small peak at 75 MHz), whereas the simulations predict a frequency of 14 MHz during the off-time (agreeing with the measurements) and 36 MHz during the on-time. In the simulations, there is also a small frequency peak at 72 MHz. However, the behaviour of the current during the on-time is clearly less well simulated than during the off-time. A possible reason for this lies in the Spice model of the diode, which seems to correspond not so well with reality.

The simulated resonance frequencies of 14 and 36 MHz in the current spectrum can also approximately be calculated using the formula for the resonance frequency of an LC-circuit:

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{4.46}$$

For the on-state of the switch, the high-frequency current flows in the rectangular loop defined by the nodes N1-N2-N7-N12-N13-N14-N30-N15-N16-N17-N18-N19-N20-N21-N1 (Fig. 4.28). It passes through the capacitance between nodes N7 and N2 because this represents a low-ohmic impedance at high frequencies. The inductance of this rectangular loop can be calculated with FastHenry or measured (see next Section), but can also be calculated. Using formula (34) on page 53 of [Term 43], we find an inductance of 371.9996 nH. In the on-state of the switch, the diode is blocking the current and is essentially a capacitor. The

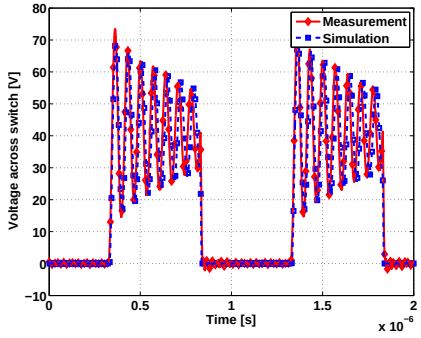
value of its junction capacitance can be found in the PSpice-model or calculated with the following formula [PSpi 00]:

$$C_J = \begin{cases} C_{J0}\,(1 - V_{pn}/V_J)^{-M} & \text{if } V_{pn} \leq FC \cdot V_J; \\ C_{J0}\,(1 - FC)^{-(1+M)}\,(1 - FC(1+M) + MV_{pn}/V_J) & \text{if } V_{pn} > FC \cdot V_J. \end{cases} \tag{4.47}$$

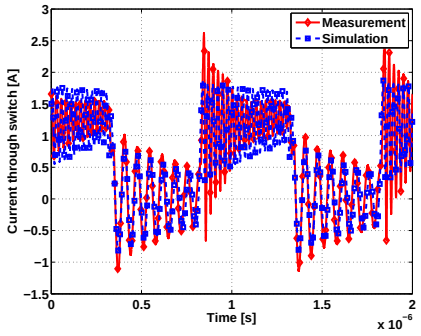
with C_{J0} the zero-bias p-n-capacitance ($C_{J0} = 260.04$ pF), M the p-n-grading coefficient ($M = 0.42769$), FC the forward-bias depletion capacitance coefficient ($FC = 0.5$), and V_{pn} the p-to-n voltage. The junction capacitance is 54 pF at a blocking voltage of 40 V. With these values, we find a resonance frequency of 35.43 MHz, which is close to the simulated value of 36 MHz.

During the off-state of the switch, the high-frequency switch current is not zero as can be seen in Fig. 4.31b but shows a lot of ringing. The switch blocks this time and is represented by a capacitor. This capacitor is the output capacitor C_{oss} of the MOSFET and its value is found in the datasheet and is about 380 pF at 40 V. This predicts, together with the same inductance value, a resonance frequency of 13.3862 MHz, which is close to the simulated value of 14 MHz.

However, PCB-circuits do not always have geometries for which analytical formulas can be applied to calculate inductance values and the PEEC-method is therefore a very useful tool.



(a) Measured and simulated voltage across the switch of the reversed buck converter.



(b) Measured and simulated current through the switch of the reversed buck converter.

Figure 4.31: Switch voltage and current of the reversed buck.

The most important conclusion that we draw from these simulations and measurements, is the fact that the exact layout of the PCB-tracks is of great importance for the behaviour of voltages and currents when fast changing (pulse) voltage excitations occur. It is seen that where ideally the voltage across the switch is 40 V when it is off, in the real case, because of the interaction of the PCB-track parasitics with the components parasitics, the voltage now swings

up to almost double this value: 73 V! Care must thus be taken to make the size of the switching cell as small as possible.

4.5.6 Inductance of the switching cell of the reversed buck

The switching cell is the part of the converter between the input capacitor, the diode and the switch. For the case of the reversed buck, it is the -almost square- cell between C_{s2}, D_1 and M_1. The switching cell of a converter should be as small as possible, because in that case, not too much energy is stored in the loop. Then, the diode or switches are not subjected to a high voltage when they switch off, because the energy of this loop has to be transferred to their capacitances. The inductance of the switching cell resonates with the capacitance of the diode or switch when they are off, producing ringing on the voltage and current waveforms. The PEEC-method can be used to determine this inductance. If the inductance is known and the frequency of the ringing phenomenon can be measured, the capacitance of the diode and switch can then be determined. Therefore, it is useful to know the inductance of the switching loop. The PEEC-method can be useful in that respect. The shunts R_1 and R_2 and the diode D_1 and transistor M_1 are short circuited, and the PEEC-simulation gives an inductance of 326.35 nH at 1 MHz. It is almost exactly a perfect inductance, because the phase difference between voltage and current is 89.9978 degrees. As a comparison, the inductance is also measured, and the measurement value is 334.22 nH. The error is hence very small: (334.22-326.35)/334.22=2.36%.

4.5.7 Current the input capacitance has to deliver

We want to know what current the input capacitance C_{s2} has to deliver to feed the switching cell inductance. Thereto, the frequency spectrum of this current is compared with the current through C_{s2} when all the copper tracks are ideal: zero length and zero impedance. The results are shown in Fig. 4.32. It can be seen that a much higher current has to flow from the input capacitance in reality than in the ideal case, in the frequency range from 230 kHz to 17 MHz. For higher frequencies, different resonances exist in the ideal case and in the real case, where sometimes, neighbouring resonances have equal current magnitudes. However, over the complete frequency range, the average current is 0.42 mA for the ideal case and is more than double, 0.96 mA for the case where the PCB-tracks are modelled. This shows that PEEC-simulations can also play an important role in dimensioning input capacitances and this shows an immediate practical application of the method.

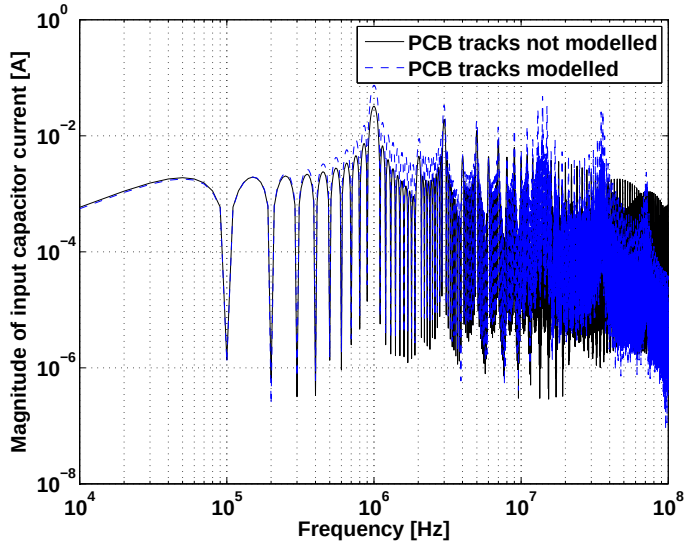


Figure 4.32: Currents through the input capacitor C_{s2} of the reversed buck when all connections are real PCB tracks or when these are ideal.

4.6 Simulating a long and thin coupled transmission line

4.6.1 Geometry, subdividing in inductive and capacitive segments

A coupled transmission line (TL) with a large aspect ratio is modelled as a 3D-structure. The purpose of this test is to see how the method copes with such large aspects ratios. The TL consists of two parallel, copper conductors (length $l = 50$ mm, width $w = 20$ μm, and thickness $t = 1$ μm) which are separated at a distance $d = 20$ μm from each other (Fig. 4.33). Each of the conductors is uniformly discretized with 20 subdivisions along its length direction. The frequency at which the skin-effect is calculated is 333 MHz. No substrate is present. A bipolar junction transistor (BJT) of which the collector output is connected to the transmission line and a load, is used for the drive circuitry. The BJT is operating as a common-emitter switch. The aspect ratio is the ratio $l/t = 50/(1 \cdot 10^{-3}) = 50000$.

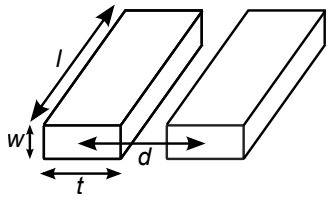


Fig. 4.33: Geometry and dimensions of the coupled transmission line with the large aspect ratio.

4.6.2 Using Spice to simulate the voltage and current waveforms

The self- and mutual partial inductances, the self-resistances (mutual resistances are not used in this work), and the self- and mutual partial capacitances are inserted in a Spice subcircuit (.SUBCKT) modelling the PCB-tracks, with respectively the Spice elements L, K, R, C and C. PSpice is used as Spice simulation tool. The subcircuit modelling the PCB-tracks is imported and the external resistors, capacitors and transistor are connected, together with the input voltage source (Fig. 4.34). The transistor is a 2N2222 BJT transistor.

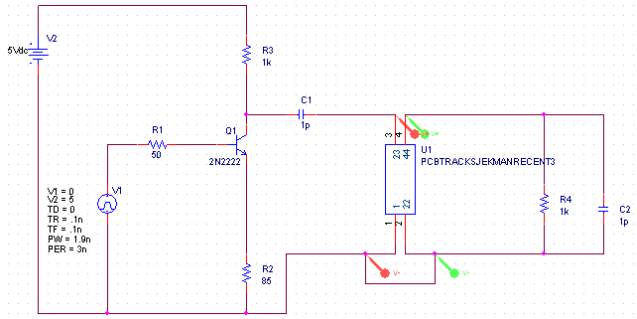
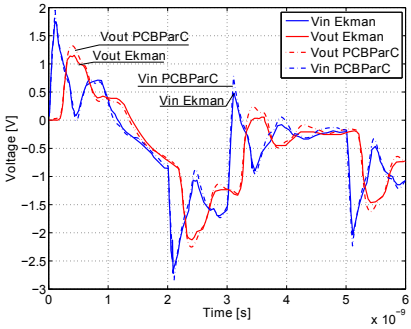


Figure 4.34: Importing the model for the PCB-tracks of the coupled TL driven by a BJT into Spice.

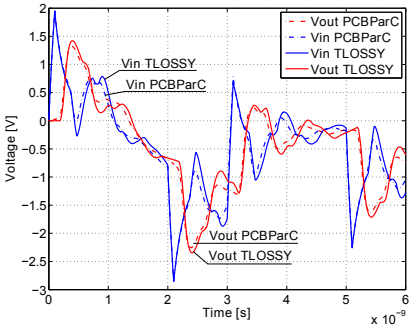
4.6.3 Results

The input and output voltage of the transmission line is calculated in PSpice. The simulations of this work, denoted by 'PCBParC', are compared to the results obtained by the 3D PEEC method developed by Prof. Jonas Ekman of Luleå University, Sweden [Ekma 03][Safa 11]. In Ekman's work, also a circuit

solver is developed, able to solve delay-differential equations. The results are presented in Fig. 4.35a. An very good agreement is noticed, indicating that the method of this work is able to cope with large aspect ratios in the inputted geometries.



(a) Simulated voltages at the input and output of the TL.



(b) Comparing the results from the simulation using the method of this work with the results of the Spice simulation with the TLOSSY model.

Figure 4.35: Simulated voltages at the input and output of the TL, (a) using PEEC-methods, (b) comparison with Spice's TLOSSY model.

These results are compared with the Spice simulation where a model for a lossy transmission line (TLOSSY) is used (Fig. 4.36). We have for the characteristic impedance (for $w/h > 1$, with $h = d - t$) [Paul 06]:

$$Z_c = \frac{377}{\sqrt{\epsilon_r}\left(\frac{w}{h} + 0.441 + \frac{\epsilon_r+1}{2\pi\epsilon_r}\left(\ln\left(\frac{w}{h} + 0.94\right) + 1.451\right) + 0.082\frac{\epsilon_r-1}{\epsilon_r^2}\right)} \tag{4.48}$$

The per unit length capacitance and inductance are

$$C = \frac{1}{vZ_c} \qquad \text{and} \qquad L = \frac{Z_c}{v} \tag{4.49}$$

where $v = c/\sqrt{\epsilon_r}$ and c is the speed of light. With these formulae, and $\epsilon_r = 1$, we find for the transmission line $Z_c = 173.3365\ \Omega$, $L = 577.79$ nH/m, $C = 19.230$ pF/m. The DC resistance per unit length is $R_{DC} = 1/(t \cdot w \cdot 5.8108 \cdot 10^7) = 860.4667\ \Omega$/m and the conductance G is 0 S/m. Also, TLOSSY requires the electrical length of the transmission line, LEN. Because the switching frequency of the BJT is 1/(3 ns)=333 MHz, the corresponding wavelength is $\lambda = c/(333 \cdot 10^6)$ and LEN is $50 \cdot 10^{-3}/\lambda = 0.0555$.

Again, it can be seen that the method of this work, using a quasi-static PEEC-method, agrees well with the method used by the TLOSSY model of Spice for simulating transmission lines.

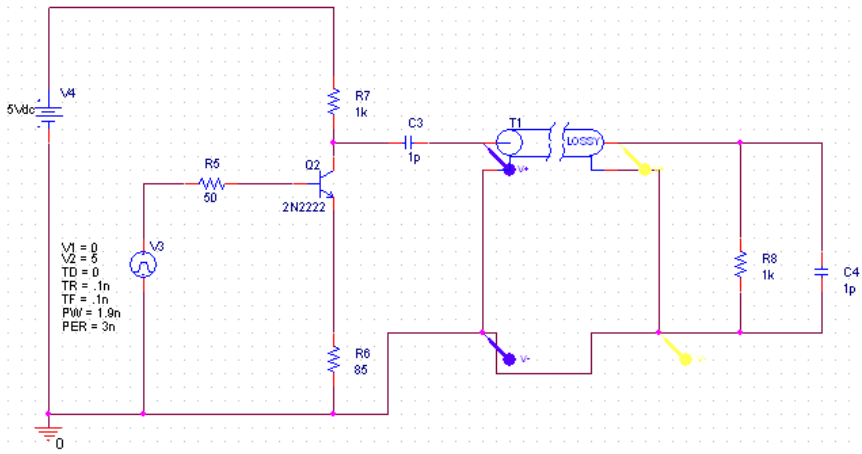
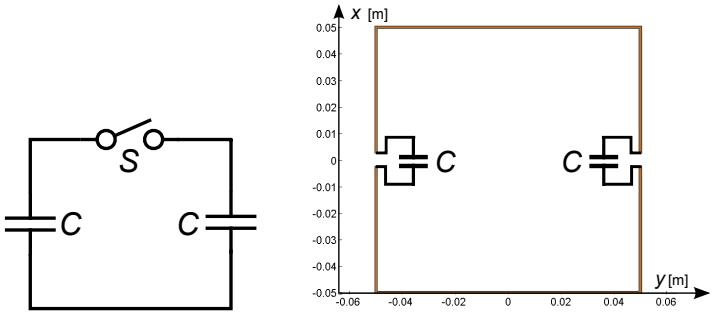


Figure 4.36: Simulating the transmission line with the TLOSSY model of Spice.

4.7 Two-capacitor problem

4.7.1 Description of the problem

The two-capacitor problem involves a circuit containing two equal capacitors C which are connected in parallel with perfectly conducting wires. Furthermore, there is an ideal switch S between the two capacitors (Fig. 4.37a). First, the switch is open. One of the capacitors is charged and has a voltage V. The other one is not charged. Then, the switch closes. After a transient, the voltage across the two capacitors is equal to $V/2$. However, the energy in the system before the switch closes is $CV^2/2$, and it is $2C(V/2)^2/2 = CV^2/4$ after the switch closes. The energy before and after the operation of the switch is not the same. Where did the rest of the energy go to? In literature [McDo 02][Boyk 02] it is explained that the rest is radiated, or equivalently said, dissipated in the radiation resistance. In this Section, the problem is assessed with the PEEC-method. A quasi-static technique is first used. Then, no radiation resistance is included in the model for the electrical circuit (for perfectly conducting wires, the only elements in the model are self- and mutual inductances and capacitances) and radiation is not modelled. In Section 4.7.5 it will be shown that a full-wave model is ill-conditioned and therefore is difficult to use for determining the radiation effects quantitatively.



(a) Two-capacitor problem. (b) Geometry and dimensions of the two-capacitor problem.

Figure 4.37: Two capacitor problem and the dimensions of the geometry.

4.7.2 Geometry and subdivision in inductive and capacitive segments

Two capacitors of 1 μF each are connected with each other via perfectly conducting wires, laid out in a square pattern (Fig. 4.37b) where each edge of the square has a length of 10 cm. There is no substrate present. The wires have a square cross-section of 1x1 mm^2. There are two 'gaps' of length 5 mm in the square where the capacitors are placed. There is no switch present in this Figure, but this poses no problem as will be shown in the next Section.

4.7.3 Using Spice to simulate the voltage and current waveforms

The self- and mutual partial inductances and the self- and mutual partial capacitances are inserted in a Spice subcircuit (.SUBCKT) modelling the PCB-tracks, with respectively the Spice elements L, K, C and C. PSpice from Cadence [Cade] is used as Spice simulation tool. The subcircuit modelling the PCB-tracks is imported together with the external capacitors, switch and the input voltage source (Fig. 4.38). The switch is an ideal Spice element S. It has an off-resistance of 100 MΩ and an on-resistance of 10^{-10} Ω. It is voltage-controlled and switches between the on- and off-state when the voltage exceeds 5.1 V or falls below 5 V. First, the left capacitor is charged to 12 V and after 1 microsecond, the switch is closed and the two capacitors are connected to each other.

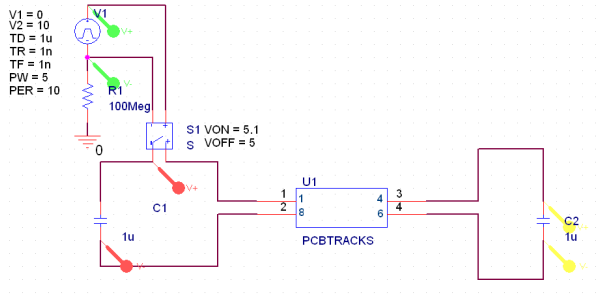


Figure 4.38: Importing the model for the PCB-tracks of the two-capacitor problem into Spice.

4.7.4 Results

The voltages across the two capacitors are shown in Fig. 4.39. After the switch closes, they continue oscillating and never reach a constant value of $V/2 = 6$ V, as occurs in reality, indicating that the quasi-static method of this work is not able to cope with radiation phenomena.

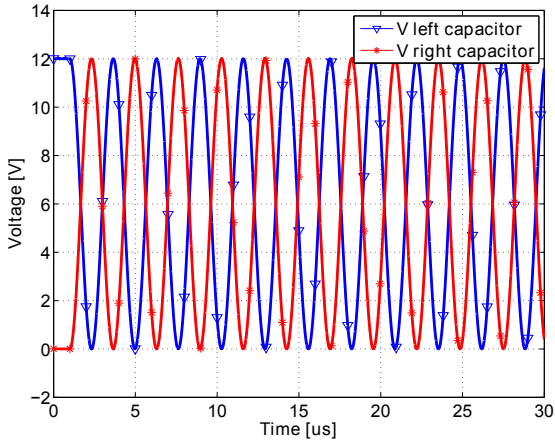


Figure 4.39: Voltages across the two capacitors, simulated with a quasi-static approach.

4.7.5 Full-wave analysis of the two-capacitor problem

A full-wave analysis of the two-capacitor problem is set up, but the simulation did not converge. A full-wave equivalent model with voltages sources was used, and when that did not converge, a model with current sources was used.

Stabilizing schemes with the R-ind and the R-cap methods were used (see Section 4.3.9), as well as several different topologies, segmentations and capacitance values for the two-capacitor problem, but no convergence was obtained. Also copper wires instead of perfectly electrically conducting wires were used, at the same time making sure that the theoretical radiation resistance value was much higher than the conduction resistance. Finally, different PSpice solvers, step sizes, and methods to improve convergence (such as GMIN stepping) were tried, but none of these resulted in correct results. It was also attempted to start from the theoretical final solution, and then investigate if the system would remain in this final state, but a late-time divergence was observed.

The reason for these convergence problems lies in the fact that the two-capacitor system is ill-conditioned. The frequency-dependent system matrix $M(s)$ (see Section 4.3.8) is determined and the condition number is calculated. This is a measure for the relative error on the state vector, when there are perturbations in the system matrix. Mathematically, the system is described by (see eq. (4.29)):

$$[M(s)][X] = [Y] \tag{4.50}$$

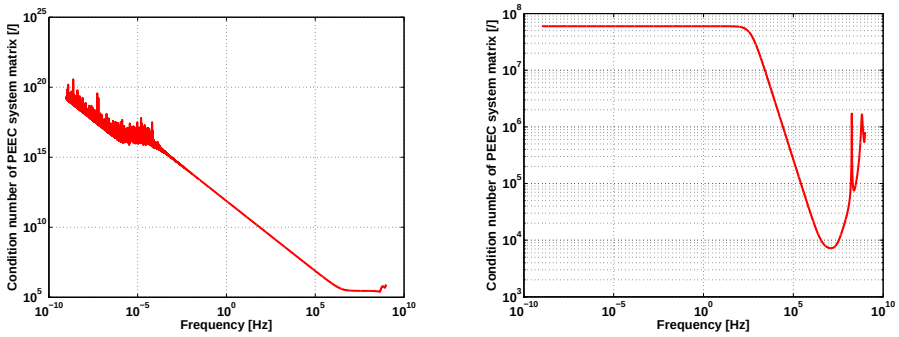
with $[X]$ the state vector, $[M(s)]$ the system matrix and $[Y]$ the vector of the excitations. If there are perturbations $[\Delta M(s)]$ on the system matrix so that the following holds [Bult 06]:

$$[M(s) + \Delta M(s)][X + \Delta X] = [Y] \tag{4.51}$$

then the perturbations on $M(s)$ get blown up with the condition number of the system matrix, $\kappa(M(s))$:

$$\frac{||\Delta X||}{||X||} \leq \kappa(M(s)) \frac{||\Delta M(s)||}{||M(s)||} \tag{4.52}$$

Moreover, if $\kappa(M(s))$ is of the order 10^k, you lose k significant digits in the calculation of the state vector. Therefore, as a rule-of-thumb, condition numbers of over 10^{18} are not acceptable anymore. The condition number of the system matrix of the two-capacitor problem (Fig. 4.40a) is compared with that of the resistance-divider network of Section 4.4.1 (Fig. 4.40b). It can be seen that the condition number of the resistance-divider network is several orders of magnitude smaller. The condition number of the two-capacitor problem becomes unacceptably large for frequencies under 1 Hz. The two-capacitor problem is therefore ill-conditioned at low frequencies and a full-wave solution is difficult to obtain.



(a) Two-capacitor problem. (b) Resistance-divider problem.

Figure 4.40: Condition numbers of the system matrix of two PEEC problems.

4.8 Currents along a simple transmission line

A final verification of the developed full-wave PEEC-technique, is given in the problem of a two-wire transmission line, depicted in Fig. 4.41. The line consists of two lossless wires with a square cross-section. The dimensions of the line are: $L = 0.5$ m, $s = 20$ mm and $w = 2$ mm. The line is attached to a sinusoidal voltage source V_{in} with amplitude 1 V and the other end is left open. Transmission line theory learns that the amplitude of the currents along the x-axis is given by [Carl 98]:

$$I(x) = \frac{V_{in}}{Z_c\left(1 + \Gamma_L e^{-j2L\beta}\right)}\left[e^{-jx\beta} - \Gamma_L e^{j\beta(x-2L)}\right] \tag{4.53}$$

where V_{in} is the amplitude of the input voltage source, β is the phase constant, Γ_L is the reflection coefficient at the right end of the line and Z_c is the characteristic impedance of the line. It is given by:

$$Z_c = 120 \cdot \ln\left(\frac{4s}{w}\right) \tag{4.54}$$

Because of the open right end, the reflection coefficient is $\Gamma_L = 1$. A full-wave

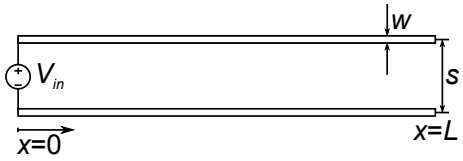


Figure 4.41: Description of the simple transmission line geometry.

PEEC-simulation was carried out, using 30 inductive segments per wire, and with a size of the capacitive panels equal to w. The amplitude of the current wave along the line is calculated for three frequencies, 10, 50 and 300 MHz. The results are shown in Fig. 4.42. It can be seen that the current has a standing wave-like behaviour, and that a full-wave analysis of the problem is necessary. The simulated curves approximate the theoretical curves very well, for 10 and 50 MHz. At 300 MHz, the structure will resonate, because the length of the line is equal to half a wavelength. The input impedance of the line varies very steeply around the resonance frequencies and therefore, the PEEC-analysis at 300 MHz corresponds to a theoretical analysis at 315 MHz. An important conclusion can thus be drawn: the PEEC-method of this work is reliable except when systems resonate: the exact behaviour around resonance is badly conditioned, meaning that it is highly dependent on the exact value of the used frequency. Nevertheless, the system behaviour at the resonance frequency predicted by the PEEC-method resembles well the system behaviour at the real resonance frequency, as is discussed in the next Chapter.

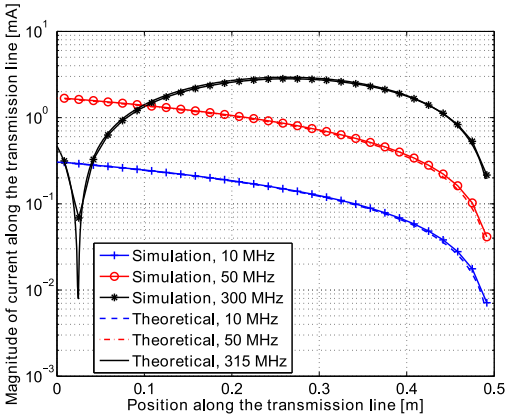


Figure 4.42: Currents along the axis of the simple transmission line geometry.

4.9 PCBParC

A software tool, PCBParC -for PCB Parasitics Calculator- is developed implementing the method of this work. It runs on Windows PCs, is developed in Matlab, and uses Visual Basic Script together with the Windows Automation API to call FastHenry and FastCap. Windows-implementations of FastHenry and FastCap can be freely downloaded from [Fast]. Only rectangular PCB-tracks are allowed, which are either parallel or perpendicular to each other. Furthermore, they must be located in a plane, parallel to the xy-plane. A

dielectric substrate immediately underneath the tracks or at a certain distance under them, can be included. Also, it is possible not to have a substrate present in the structure. One can choose to do a quasi-static or full-wave simulation, but in the full-wave simulation, the substrate is neglected. Also the skin- and proximity-effects are taken into account, but in a *global* way; that means: the total conductor resistance is determined taking the skin- and proximity-effects into account. In order to run the programme, the Matlab Compiler Runtime (MCR) must be installed or the user must have a version of Matlab installed on his computer. PCBParC produces a file containing the Spice-subcircuit of the inputted PCB-tracks. The programme can be freely downloaded from [PCBP]. More information about its use and the underlying principles can be found in its manual (see Appendix I).

4.10 Conclusion

In this Chapter, a method is outlined for accurately simulating the parasitic elements of power electronic converters. Switching components consist of semiconductor blocks of specific dimensions and these blocks are often connected with the component's terminals via bonding wires. These switching components are connected with other components through copper tracks on a PCB-circuit. These wires and tracks and the internal semiconductor block connections have resistance, capacitance and inductance, but those are unintendedly present. These parasitics become more dominant when the switching frequency increases or when the rising or falling edges of current or voltage waveforms decrease. This work investigates power convertors operating at high switching frequencies and at fast speeds, and at these speeds, parasitic effects can become problematic and it is good to predict them with accurate models. The reason that parasitics become more of an issue at high dv/dt or di/dt is that capacitances have an impedance being inversely proportional to the frequency and inductances have an impedance being directly proportional to the frequency. Therefore, parallel parasitic capacitances will draw more current at higher frequencies and series parasitic inductances will block more current. Also, the energy stored in these parasitics during each switching period becomes of the same order as the useful energy, which is normally transferred per switching operation in a converter without parasitics.

In the doctoral work of Bolsens, wire parasitics are analyzed with the Method of Moments, operating in the frequency-domain and involving complex calculations. In this work, another method is used. It is called the Partial Element Equivalent Circuit (PEEC) method. It models PCB-tracks with a network of lumped elements which then can be an input for a Spice-like circuit solver together with the Spice-models of the switches and other converter components and which can be solved in the time-domain or frequency-domain.

First, a converter containing only linear elements, a resistance-divider circuit, is analyzed, and next, a switched-mode power supply is taken as an example. The used partial element equivalent circuit method is quasi-static. It is used to simulate the step response and the voltage and current waveforms in the converter in the presence of parasitics, validating the method. The freeware programmes FastHenry and FastCap are used, calculating the partial elements very efficiently. The method also allows a dielectric substrate to be present in the circuit structure, lying underneath the copper tracks, and modifying the matrix of the partial capacitances.

The input impedance of the resistance-divider circuit is calculated in function of the frequency and compared with Method of Moment calculations, up to gigahertz frequencies. For this purpose, the quasi-static method has to be extended into a full-wave version, employing delayed voltage or current sources to model propagation delays. In order to solve circuits with delayed sources in Spice, use was made of the LAPLACE-directive.

To validate the capacitance extraction technique, the capacitance per unit length of a structure of two parallel tracks on a substrate is calculated with the PEEC-method and the results are compared with Finite Elements calculations and analytical results.

Also the waveforms in a fast switching common-emitter BJT-amplifier circuit, connected to a two-wire transmission line with a high aspect ratio, are calculated and compared with other simulation results. A good agreement is observed.

Another full-wave verification experiment is next set up: the currents along the length of a transmission line are calculated with the method of this work and compared with the theoretical values. A good agreement is observed, except around the resonance frequency. There, the impedance has a very steep behaviour as function of the frequency and small frequency deviations give large differences in the observed phenomena. However, at the simulated resonance frequency, where the imaginary part of the input impedance is zero, the behaviour is the same as at the theoretical resonance frequency.

In Matlab, a tool for parasitics extraction is developed. It is called PCBParC and can be freely downloaded from the Internet. It uses FastHenry and FastCap and extracts a PEEC-equivalent circuit (quasi-static or full-wave) from the PCB-tracks of a converter and produces a Spice-netlist for it. The manual of this software programme is given in Appendix I.

The value of this work is that a freeware PEEC-simulator has been created, which uses FastHenry and FastCap to calculate the partial elements. FastHenry and FastCap are already highly computationally efficient so implementing a dedicated method to calculate the partial elements was not deemed necessary. Furthermore, Spice is used to solve the obtained circuits. All Spice flavours that can deal with LAPLACE-directives can solve the full-wave models.

5

Electromagnetic Fields Surrounding a Power Electronic Circuit

5.1 Introduction

As was explained in previous Chapter, the parasitics of a circuit can cause problems for the signal integrity, can subject circuit components to high electrical stress and can create unwanted oscillations in the voltage and current waveforms. These oscillations are due to a resonance between the inductive PCB-tracks and other inductive components on the one hand and the parasitic capacitances of diodes and switches or of other components on the other hand. Energy is exchanged between the capacitive and inductive elements and is stored in the electromagnetic field around these elements.

This field is fluctuating in intensity and may disturb other sensitive electronic equipment in the vicinity. Also, it is possible that some part of the energy is radiated and therefore lost. In order to accurately model wave phenomena, the full-wave Maxwell's equations must be solved. They can easily be solved in the

frequency domain, as was done in Bolsens's work [Bols 05]. However, in order to also model the start-up phenomena of power converters, a time-domain solution technique usually provides an easier approach. In this Chapter, a solution is sought for the problem of calculating the electromagnetic field around power converters. The time-domain solution is given by Jefimenko's equations. They will be studied in the next Section.

The techniques of this Chapter can be used to check whether a designed power converter complies with the EMC-regulations for radiated emissions or radiated susceptibility. It makes it possible to avoid having expensive measuring equipment such as antennas, an anechoic chamber and a network analyzer or order tests in a specialized laboratory. The work thus has an immediate practical applicability and is of significant economic value as well. The frequency band for radiated emissions according to the European EMC-regulation EN 55022 starts at 30 MHz. Upcoming multi-megahertz converters, facilitated by the wide-bandgap components, introduced in Chapter 2, or by the soft-switching strategies, explained in Chapter 3, have switching frequencies of the order of 1, 10 or even 100 MHz [Pila 09][Pila 07][Riva 06] and they will therefore radiate a significant amount of power in their frequency band. They have to be designed with care so that the EMC-regulations are not violated.

5.2 Electromagnetic fields in the time-domain: Jefimenko's equations

Jefimenko's equations, according to [Grif 99] first explicitly published by the Ukrainian physicist Oleg Jefimenko (Олег Дмитрович Ефименко) (1922-2009), state the relationship between electric charge and current on the one hand and the electromagnetic fields on the other. The equations are time-domain expressions. A derivation can be found in Appendix J. A similar derivation as the one presented there can be found in [Grif 99]. The two Jefimenko equations are:

$$\boxed{\vec{E}(\vec{r},t) = \frac{1}{4\pi\epsilon}\int_V \left[\frac{\rho(\vec{r'},t_r)}{R^2}\vec{e}_R + \frac{\frac{\partial\rho}{\partial t}(\vec{r'},t_r)}{vR}\vec{e}_R - \frac{\frac{\partial\vec{J}}{\partial t}(\vec{r'},t_r)}{v^2R}\right]dV'} \tag{5.1}$$

$$\boxed{\vec{B}(\vec{r},t) = \frac{\mu}{4\pi}\int_V \left[\frac{\vec{J}(\vec{r'},t_r)}{R^2} + \frac{\frac{\partial\vec{J}}{\partial t}(\vec{r'},t_r)}{vR}\right]\times\vec{e}_R dV'} \tag{5.2}$$

The reader is referred to Appendix J for an explanation of the used symbols. The two Jefimenko equations are the dynamic generalizations of the static Coulomb's law and Biot-Savart's law, respectively.

5.3 Electromagnetic fields in the frequency-domain

In the frequency-domain, the electric field and magnetic induction can be easily expressed in terms of the scalar and vector potential (Note: eqs. (J.1), (J.2), (J.3) and (J.4) give the corresponding time-domain expressions):

$$\vec{E}(\vec{r}) = -\vec{\nabla}\phi(\vec{r}) - j\omega\vec{A}(\vec{r}) \tag{5.3}$$

$$\vec{B}(\vec{r}) = \vec{\nabla} \times \vec{A}(\vec{r}) \tag{5.4}$$

$$\phi(\vec{r}) = \frac{1}{4\pi\epsilon}\int_V \frac{\rho(\vec{r'})e^{-\gamma R}}{R}dV' \tag{5.5}$$

$$\vec{A}(\vec{r}) = \frac{\mu}{4\pi}\int_V \frac{\vec{J}(\vec{r'})e^{-\gamma R}}{R}dV' \tag{5.6}$$

where γ is the propagation constant. It is a complex number, consisting of a real part (the attenuation factor α (unit: Np/m)) and an imaginary part (the phase factor β (unit: rad/m)):

$$\gamma = \alpha + j\beta \tag{5.7}$$

The other symbols are explained in Appendix J. If the propagation of electromagnetic fields in air is considered, there is no loss or attenuation and $\alpha = 0$. In Chapter 4, an electrical circuit was subdivided in N_{ch} charge elements and N_{cu} current elements. We then have for the phasors of the electric field and the magnetic induction in a point $\vec{r}$ around the circuit:

$$\begin{aligned}
\vec{E}(\vec{r}) &= -\tfrac{j\omega\mu}{4\pi}\textstyle\sum_{n=1}^{N_{cu}}\tfrac{I_n}{A_n}\left(\int_{V_{cu,n}}\tfrac{e^{-j\beta R}}{R}dV'\right)\vec{e}_{l,n} \\
&\quad -\tfrac{1}{4\pi\epsilon}\textstyle\sum_{n=1}^{N_{ch}}\rho_n\left[\int_{V_{ch,n}}\vec{\nabla}\left(\tfrac{e^{-j\beta R}}{R}\right)dV'\right] \\
\vec{B}(\vec{r}) &= \tfrac{\mu}{4\pi}\textstyle\sum_{n=1}^{N_{cu}}\tfrac{I_n}{A_n}\left[\int_{V_{cu,n}}\vec{\nabla}\times\left(\tfrac{e^{-j\beta R}}{R}\vec{e}_{l,n}\right)dV'\right]
\end{aligned}$$

Making use of some vector calculus identities, we find:

$$\boxed{\begin{aligned}
\vec{E}(\vec{r}) &= -\tfrac{j\omega\mu}{4\pi}\textstyle\sum_{n=1}^{N_{cu}}\tfrac{I_n}{A_n}\left(\int_{V_{cu,n}}\tfrac{e^{-j\beta R}}{R}dV'\right)\vec{e}_{l,n} \\
&\quad -\tfrac{1}{4\pi\epsilon}\textstyle\sum_{n=1}^{N_{ch}}\rho_n\left[\int_{V_{ch,n}}\left(-\tfrac{1}{R}-j\beta\right)\tfrac{e^{-j\beta R}}{R}\vec{e}_R dV'\right]
\end{aligned}} \tag{5.8}$$

$$\boxed{\vec{B}(\vec{r}) = \frac{\mu}{4\pi}\sum_{n=1}^{N_{cu}}\frac{I_n}{A_n}\left[\int_{V_{cu,n}}\left(\frac{1}{R}+j\beta\right)\frac{e^{-j\beta R}}{R}(\vec{e}_{l,n}\times\vec{e}_R)dV'\right]} \tag{5.9}$$

In deriving these frequency-domain equations, it is assumed that the current of each element is flowing in one direction and that it is furthermore constant in this element. This direction has a unit vector $\vec{e}_{l,n}$. For the n^{th} element,

this constant current is I_n, and it is flowing in a direction parallel with the unit vector $\vec{e}_{l,n}$. The n^{th} element has a cross-section A_n. Also, for each n^{th} charge element, it is assumed that the charge density is constant and equal to ρ_n. $\vec{e}_R = \vec{R}/R$ is the unit vector in the direction $\vec{R} = \vec{r} - \vec{r'}$.

5.4 Electric and magnetic field between two parallel wires

In order to validate the technique of calculating electromagnetic fields, developed in this Chapter, the method is applied to a specific problem, that of the fields around two infinitely long cylindrical perfectly conducting wires, carrying a DC-current. An analytical solution is first sought and this is compared with the results of the numerical method of this Chapter.

5.4.1 Problem description

Two cylindrical wires, each conducting a DC-current I, having a radius a, are parallel to the z-axis (Fig. 5.1). They are infinitely long. The first wire is located at $x = -d$ and conducts the current in the positive z-direction. The other wire is located at $x = d$ and conducts the current in the negative z-direction. The left wire has a potential $-V_1$ and the potential on the right wire is V_1. The scalar potential, the electric and the magnetic field in the region outside the conductors must be determined. The cross-section of the right wire is bounded by a circle, called C_1. The electric potential ϕ is given by the Laplace equation:

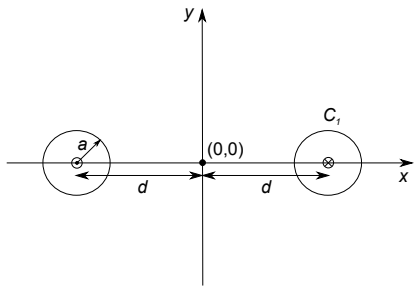


Figure 5.1: Geometry of the problem.

$$\nabla^2 \phi = 0 \tag{5.10}$$

In Appendix K, the solution is presented. The method of separation of variables is applied. The key element in solving the Laplace equation with this method is

that an appropriate coordinate system has been used: bipolar coordinates. This coordinate system allows to write the solution as a product of two single-variable functions. The solution will now be used further on. Using this analytical solution, the numerical method of this work will be (partially) validated.

5.4.2 Closed-form expressions for the scalar potential, electric and magnetic field and surface charge density

The scalar potential is:

$$\phi(x,y) = \frac{V_1}{\ln\left(\frac{d}{a} + \sqrt{\frac{d^2}{a^2} - 1}\right)} \ln \sqrt{\frac{(x + \sqrt{d^2 - a^2})^2 + y^2}{(x - \sqrt{d^2 - a^2})^2 + y^2}} \tag{5.11}$$

The electric field is:

$$\vec{E} = \frac{2(x^2 - d^2 + a^2 - y^2)\sqrt{d^2 - a^2}V_1.\vec{e}_x + 4V_1 xy\sqrt{d^2 - a^2}.\vec{e}_y}{((x + \sqrt{d^2 - a^2})^2 + y^2)\ln\left(\frac{d}{a} + \sqrt{\frac{d^2}{a^2} - 1}\right)((x - \sqrt{d^2 - a^2})^2 + y^2)} \tag{5.12}$$

The surface charge density ($[C/m^2]$) is:

$$\sigma_R = \frac{\epsilon_0 V_1 \sqrt{d^2 - a^2}}{a(d + a\cos\beta)\ln\left(\frac{d}{a} + \sqrt{\frac{d^2}{a^2} - 1}\right)} \tag{5.13}$$

For the magnetic field, the expressions are given in Appendix K. The expressions are dependent on the location of the observation point and are given by eqs. (K.38), (K.42) and (K.45).

5.4.3 Visualization of solutions

With $I = 1$ A, $V_1 = 0.5$ V, $d = 0.01$ m and $a = 0.5$ mm, the following figures depict, with some contours, the Poynting field, the electric field, the magnetic field and the scalar potential outside the wires. Also, some fieldlines of the electric field, starting on the right wire are shown, as well as the surface charge density on the surface of the right wire.

As a check, the Poynting vector was numerically integrated over the xy-plane. The field was calculated in the region for $x \in [-6d, 0]$ and for $y \in [0, 6d]$. An equidistantly spaced grid of 1000x1000 points was used. The integrated Poynting vector is then multiplied by 4 to obtain the power through the total plane. This resulted in 1.004 W, corresponding well with the theoretical value of 1 V $\times$ 1 A = 1 W.

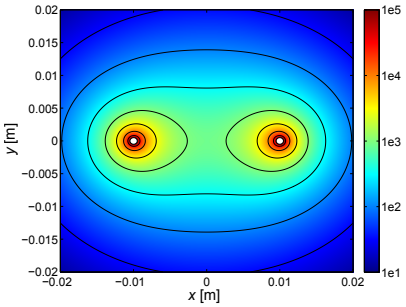


Figure 5.2: Plot of $-S_z(x, y)$.

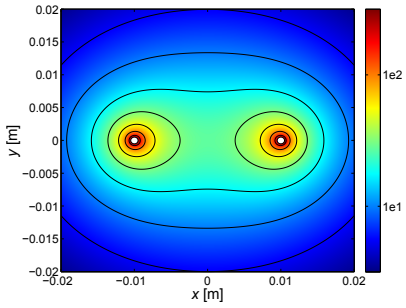


Figure 5.3: Plot of $\sqrt{E_x^2 + E_y^2}$.

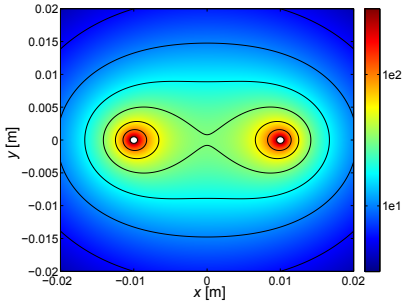


Figure 5.4: Plot of $\sqrt{H_x^2 + H_y^2}$.

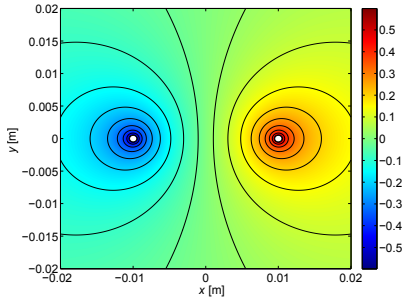


Figure 5.5: Plot of $\phi(x, y)$.

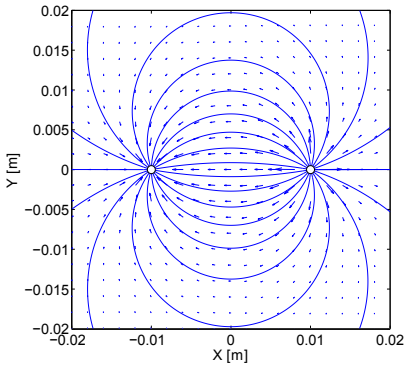


Figure 5.6: Vector and fieldline plot of $\vec{E}(x, y)$.

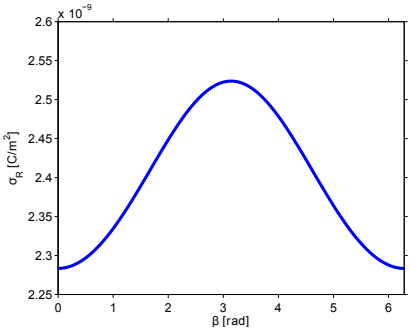


Figure 5.7: Surface charge density σ_R on the right wire

5.4.4 PEEC-simulation and calculation of fields

A quasi-static PEEC-model was used for simulating the two-wire problem and calculating the currents and charges on the wires. The geometry, material of the wires and other parameters for this PEEC-model are given in Table 5.1. The wires are not cylinders but are bars with a square cross-section, having four sides of length w. The reason that they are bars is that PCBParC only allows bar-geometries. The centre-to-centre distance of the wires is $2d$. The wires are oriented parallel to the z-axis, have each a length of l, and have the centres of their cross-section on the x-axis (Fig. 5.8).

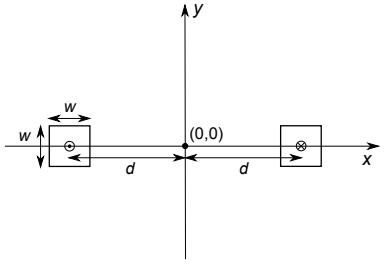


Figure 5.8: Geometry of the simulated two-wire problem

d [m]	0.01
l [m]	0.5
w [m]	$\sqrt{\pi(0.0005)^2}$
material	PEC
number of inductive segments per wire	50
size of the capacitive panels	w

Table 5.1: Parameters of the two-wire PEEC-project.

The quasi-static PEEC model was extracted with PCBParC and used in a DC-simulation in PSpice where the wires connect to a DC-voltage source of 1 V on one end to a resistive load of $R = 1\ \Omega$ on the other end. The procedure of calculating the fields is then as follows:

1. Simulate the PEEC-model in Spice, using a DC-, AC- or transient simulation (in the two-wire case a DC-simulation).
2. Extract from Spice the currents through each inductive cell and the voltages on each capacitive cell, with respect to the node '0', i.e. the space at infinite distance from the model. These currents and voltages may be functions of time if a transient simulation has been performed, or may be phasors, consisting of an amplitude and a phase when an AC-simulation has been done.
3. Calculate the charges on each capacitive cell by multiplying the vector of the voltages with the short-circuit capacitance matrix $[C_s]$, calculated by FastCap, as in eq. (4.9).
4. These charges must be modified in a next step so that the total instantaneous charge in the circuit is equal to zero. The relationship between the charge vector and the voltage vector is given by a multiplication with the short-circuit capacitance matrix: $[Q] = [C_s][V]$.

We want to modify the voltage vector so that the sum of all charges in the circuit is equal to zero at every time instance. Mathematically, this is expressed by subtracting a constant K from the voltage vector:

$$[V'] = [V] - K\,[1 \quad 1 \quad \cdots \quad 1]^T \tag{5.14}$$

This new voltage vector $[V']$ fulfills the following equation:

$$[Q'] = [C_s][V'] \tag{5.15}$$

so that the sum of all charges on each capacitive element is zero:

$$\sum_i Q'_i = 0 \tag{5.16}$$

Previous equation can also be written as:

$$[11\cdots1][Q'] = [11\cdots1][C_s][V'] = 0 \tag{5.17}$$

Inserting (5.14) into (5.17) gives, after some algebra,

$$K = \frac{\sum_i Q_i}{\sum_i \sum_j C_{s,i,j}} \tag{5.18}$$

where $C_{s,i,j}$ is the element of the short-circuit capacitance matrix on the i^{th} row and j^{th} column. This gauge parameter K should be calculated, and then, with (5.14), the modified voltage vector $[V']$ must be calculated. Next, with (5.15), the modified charges $[Q']$ must be calculated. Subtracting the constant K from the node voltages, given by Spice, is possible, because the reference potential in an electric circuit can be arbitrarily chosen. In the PEEC-step (step 1), the zero potential is chosen to lie at infinity. However, in order to impose conservation of charge, previous analysis shows that the reference potential must be modified.

5. In a fifth step, use the currents and modified charges to calculate the electric field and the magnetic induction with Jefimenko's equations (5.1) and (5.2) or with the frequency-domain equations (5.8) and (5.9).

The electric, magnetic, Poynting field and their relative procentual errors ((theoretic-simulated)/theoretic×100) as well as the electric field lines in a plane halfway the wires and perpendicular to them, are shown in Figs. 5.9-5.15. The fields are calculated in 300×250 points for $x \in [-2d, 2d]$ and for $y \in [-2d, 2d]$. The relative errors are smaller than 1 %, except for the immediate vicinity of the wires. The fields cannot be the same as the theoretical predicted in the immediate vicinity of the wires, as in the theoretical case cylindrical wires were taken and in the simulation the wires were bars. The surface integral of the z-component of the Poynting field is calculated over this plane and is equal to 0.9964 W, corresponding well with the theoretic value of 1 W. The line integral of the electric field along a straight path from the centre of the right wire to the centre of the left is 1.134 V, corresponding well with the theoretic value of 1 V.

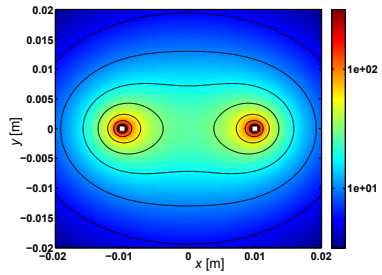


Figure 5.9: Simulated $\sqrt{E_x^2 + E_y^2}$.

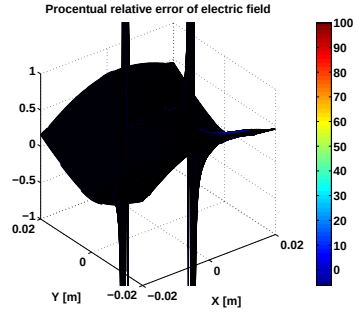


Figure 5.10: Relative procentual error of $\sqrt{E_x^2 + E_y^2}$.

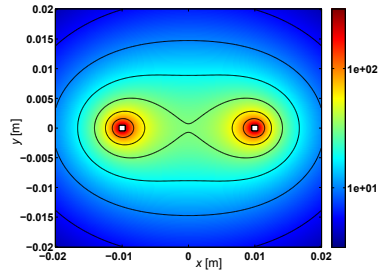


Figure 5.11: Simulated $\sqrt{H_x^2 + H_y^2}$.

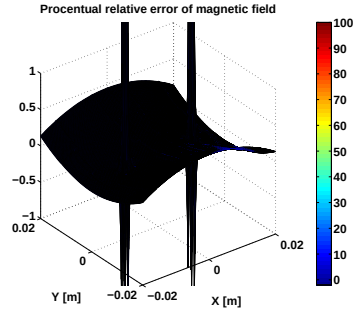


Figure 5.12: Relative procentual error of $\sqrt{H_x^2 + H_y^2}$.

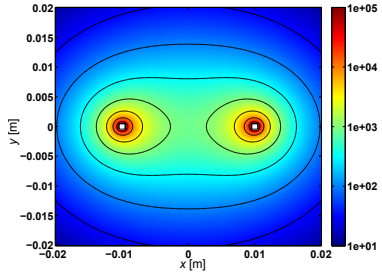


Figure 5.13: Simulated $-S_z(x, y)$.

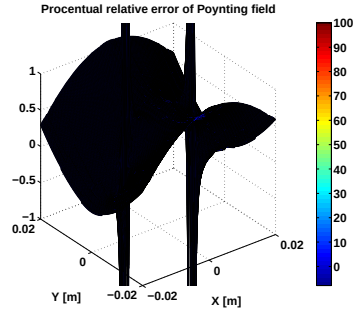


Figure 5.14: Relative procentual error of $-S_z(x, y)$.

5.5 Transient magnetic induction of an RC-circuit

In this Section, the transient magnetic induction of an RC-circuit is calculated with the method of this work, in order to validate it further. The results are compared with Comsol-simulations. Comsol [Coms] is a commercial multiphysics differential equation solver based on the finite element method. It is very user-friendly and can accurately solve boundary condition problems in the fields of electromagnetics, mechanics, chemistry, semiconductor physics, constructural engineering,... It can operate both in the time-domain and in the frequency-domain and can perform both quasi-static and full-wave electromagnetic simulations.

5.5.1 Topology and signals

The topology of the RC-circuit is shown in Fig. 5.16. All dimensions are expressed in millimetres. The tracks consist of copper and have a square cross-section of 5×5 mm^2. The resistance is $R_1 = 1\ \Omega$ and the capacitance is $C_1 = 3\ \mu$F. The voltage source produces a pulsed voltage, between $V_b = 0$ and $V_t = 10$ V, has a delay of $t_d = 2\ \mu$s, rise and fall times of $t_r = t_f = 0.1\ \mu$s, a pulse width of $PW = 9.9\ \mu$s and a period of $T = 20\ \mu$s (Fig. 5.17). The current in the circuit and the voltage across the source and capacitor are shown in Fig. 5.18. The moment where the magnetic induction is calculated (at 16 μs) is also shown.

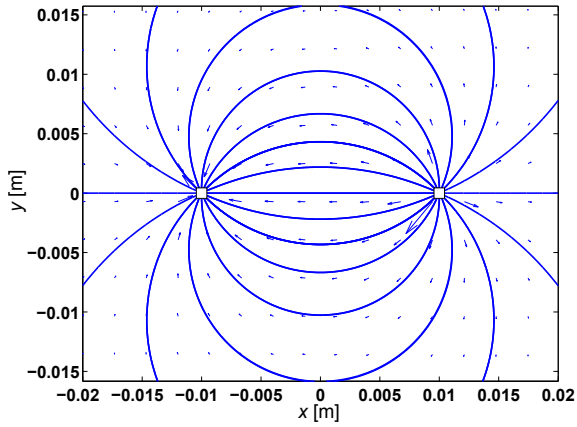


Figure 5.15: Vector and fieldline plot of the simulated $\vec{E}(x, y)$.

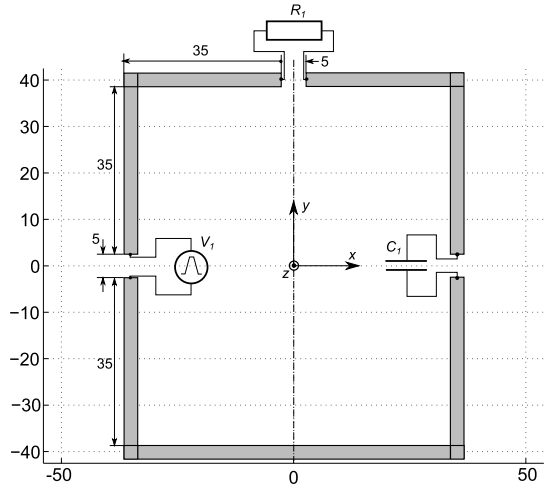


Figure 5.16: Topology of the RC-circuit; dimensions in millimetres.

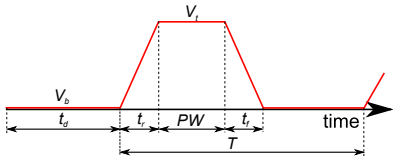


Figure 5.17: Voltage waveform of the pulsed voltage source V_1 of the RC-circuit.

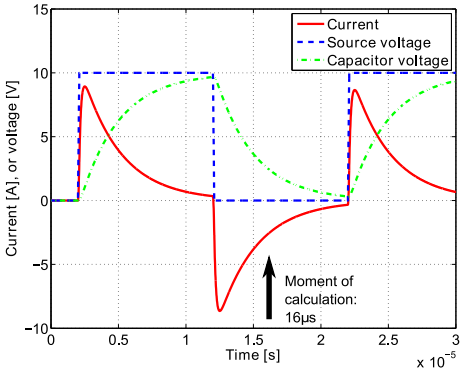


Figure 5.18: Some current and voltages in the RC-circuit.

5.5.2 Result and comparison with Comsol

At time $t = 16$ μs, the magnetic induction is calculated in a plane, parallel to the xy-plane, 5 mm above the centre of the tracks. A quasi-static modelling method is used, and the 5-step procedure of Section 5.4.4 is employed. The norm of the magnetic induction is shown in Fig. 5.19. It is compared with the quasi-static finite elements Comsol simulation (Fig. 5.20). In order to compare the two figures, some slices where made for different x-coordinates. The comparison between Comsol and the method of this work for $x = 0$ mm, is shown in Fig. 5.21, and is depicted in Fig. 5.22 for $x = -35$ mm, that means,

right above the left copper tracks. The comparison is good, but some points of interest are to be noted.

1. For the $x = 0$-slice, the two peaks are equally large with the method of this work, while Comsol gives an unequal result. This is due to the fact that the gap where the resistor is located, has to be taken out of the solution domain in Comsol, while it is included in the method of this work.

2. The Comsol-simulation of the norm of the magnetic induction right above the left tracks is not so smooth. This is simply a numeric effect, due to the sizes of the mesh elements.

3. However, the norm of the magnetic induction right above the left tracks in the Comsol-simulation is a bit lower than in the simulation with the method of this work. This is due to the skin- and proximity-effect, which are not modelled in this work but is in Comsol, and due to these effects the current mainly flows in the skin of the inside of the conductor loop.

As a conclusion, we can say that the quasi-static transient method of this work of calculating the magnetic induction is validated and is sufficiently accurate.

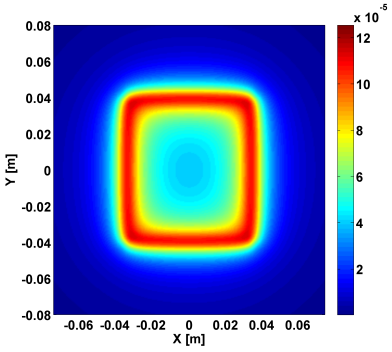


Figure 5.19: Norm of the magnetic induction, calculated with the method of this work, at $t = 16$ μs in a plane, 5 mm above the centre of the tracks of the RC-circuit.

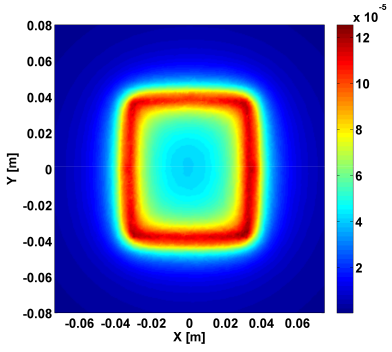


Figure 5.20: Norm of the magnetic induction, calculated with Comsol, at $t = 16$ μs in a plane, 5 mm above the centre of the tracks of the RC-circuit.

The difference in calculation speed is very large. On a 64 bit machine with 5.87 GB usable RAM and an Intel Quad CPU Q9550 with 2.83 GHz clock speed, the Comsol simulation of the magnetic induction alone (1399443 degrees of freedom, from 0 till 30 μs with a maximum step size of 100 ns) lasts 15 hours, 19 minutes and 14 seconds. These are 55154 seconds. The method of this work takes:

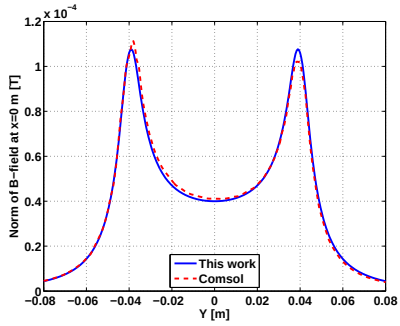


Figure 5.21: Comparison of the norm of the magnetic induction, for a slice $x = 0$ mm.

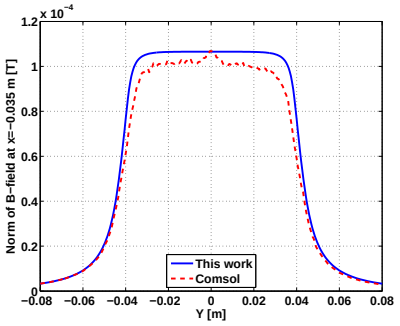


Figure 5.22: Comparison of the norm of the magnetic induction, for a slice $x = -35$ mm.

1. 363 seconds to run FastHenry, FastCap, produce the Spice-file and save the geometry.
2. 94 seconds in order to do the PSpice-simulation from 0 till 30 μs with a maximum step size of 10 ns.
3. 142 seconds in order to calculate 10000 harmonics of the currents and voltages.
4. 3730 seconds in order to calculate the electric, magnetic and Poynting fields on a 251x301-points grid.

This results in a total time of 4329 seconds.

5.6 Fields of a Yagi-antenna

5.6.1 Introduction

A Yagi-antenna (Fig. 5.23) consists of dipoles, having their centres on the x-axis and being parallel to the y-axis. The second dipole is driven, the others are parasitic, meaning that they are only electromagnetically coupled to the driven element but are not driven themselves. The first dipole has a length which is slightly longer than the length of the driven element; it is the reflector. The elements to the right of the driven element are directors. They have a length slightly smaller than the length of the driven element. The function of the reflector and the directors is to direct the radiation in a preferential direction along the x-axis. Element i has its centre at position $x = d_i$, has a length L_i and wire radius a_i.

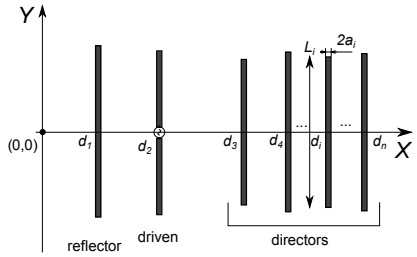


Figure 5.23: Topology of a Yagi-antenna.

w	$\sqrt{\pi a_i^2}$
material	PEC
number of inductive segments per wire	20
size of the capacitive panels	w
length of the gap in the driven element	$0.02L_2$

Table 5.2: Parameters of the Yagi PEEC-project.

5.6.2 Currents and charges of a three element Yagi-antenna

In this Section, a three element Yagi-antenna is examined, with dimensions in wavelengths:

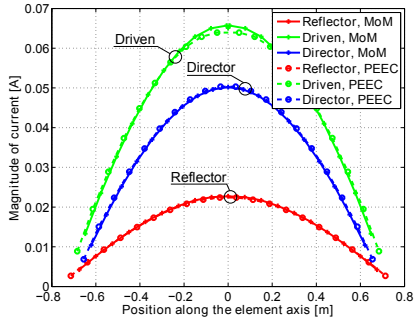
$$[L] = \begin{bmatrix} L_1 \\ L_2 \\ L_3 \end{bmatrix} = \begin{bmatrix} 0.5 \\ 0.48 \\ 0.46 \end{bmatrix} \text{ [wavelengths]} \tag{5.19}$$

$$[d] = \begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} -0.125 \\ 0 \\ 0.125 \end{bmatrix} \text{ [wavelengths]} \tag{5.20}$$

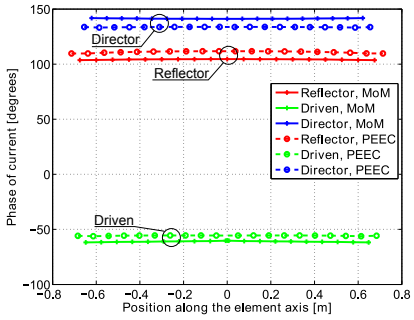
$$[a] = \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix} = \begin{bmatrix} 0.003 \\ 0.003 \\ 0.003 \end{bmatrix} \text{ [wavelengths]} \tag{5.21}$$

A full-wave PEEC-simulation was set up where each wire is modelled by a bar with a square cross-section with side w and with, besides the previous geometric data, parameters as given in Table 5.2. The wavelength for which the dimensions are determined, corresponds to a frequency of 100 MHz.

As a reference, the currents and charges along the length of the three elements are also calculated with the freeware Method of Moments (MoM) [Harr 68] [Gibs 07] based software tool MMANA-GAL [Mman]. The frequency at which these quantities are calculated, is not entirely the same in the MoM-simulation and the PEEC-simulation. In the former, it is 100 MHz and in the latter, it is 97.283 MHz. Both correspond to the resonance frequency, calculated with the respective methods. The currents and charges are calculated because they are the sources for the electromagnetic fields. As can be seen from Figs. 5.24a, 5.24b, 5.25a and 5.25b, the PEEC-simulation predicts currents and charges which are almost the same as in the reference case, but there is a phase difference of about 9° in the currents and charges of the director element.

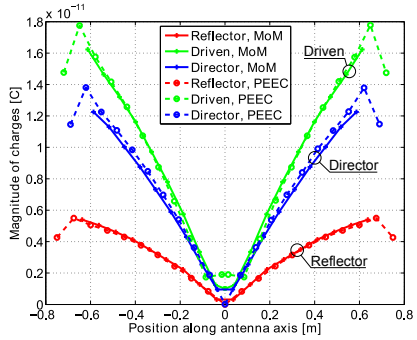


(a) Magnitude.

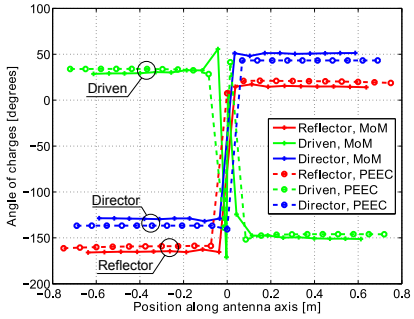


(b) Phase.

Figure 5.24: Currents along the three elements of the Yagi-antenna, calculated by MMANA-GAL and by the PEEC-method: magnitude and phase.



(a) Magnitude.



(b) Phase.

Figure 5.25: Charges on the three elements of the Yagi-antenna, calculated by MMANA-GAL and by the PEEC-method: magnitude and phase.

5.6.3 Input impedance of the three element Yagi-antenna

Also, the input impedance in function of the frequency (up to 400 MHz) is calculated with the full-wave PEEC-method (40 inductive segments per wire element), and is compared with the results produced by the Method of Moments (freeware software tool 4NEC [4nec], 61 inductive segments per wire element) and with theoretic results ([Orfa 14], ch. 23, with eqs. (23.3.7) and (23.3.8)) (Fig. 5.26 and 5.27). The theoretic input impedance is only given up to 120 MHz because to formula has singularities at and is not very accurate in the neighbourhood of wavelengths that are multiples of the length of a Yagi-element. Nonetheless, a good agreement can be observed between the three curves. The frequency range is from DC up to 400 MHz because 40 segments are used per

wire element in the PEEC-simulation and, as a rule of thumb, 20 segments are needed per wavelength in order to be able to use the approximation that the current is constant on each segment. The resonance frequency, i.e. the frequency where the phase of the input impedance is zero and the antenna is purely resistive, radiating all of the power which is supplied to the antenna, is 98.12 MHz for the MoM-simulation, 99.82 MHz theoretically and is 100.8 MHz for the PEEC-simulation.

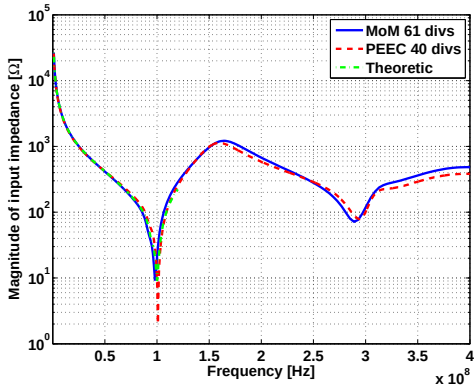


Figure 5.26: Magnitude of the input impedance of the Yagi-antenna.

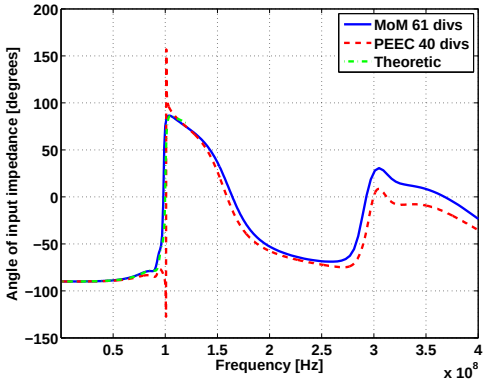
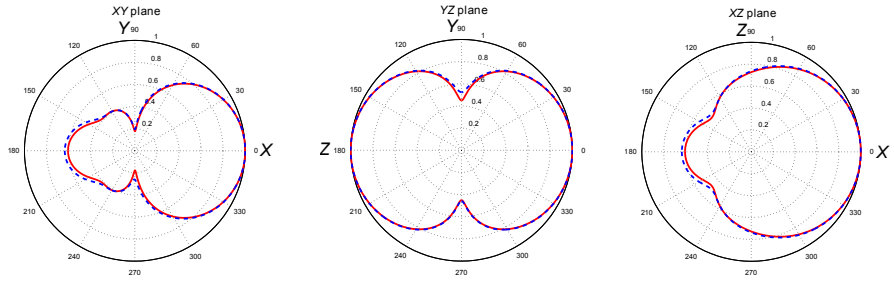


Figure 5.27: Phase of the input impedance of the Yagi-antenna.

5.6.4 Far field of the three element Yagi-antenna

The magnitude of the far electric field at 100 MHz of the Yagi-antenna in the xy-, yz- and xz-planes are shown in Figs. 5.28a, 5.28b and 5.28c. 20 segments are used per wire element. The solid line is the MMANA-GAL result (MoM)

and the dashed line is the result of the work of this doctoral work (eqs. (5.8) and (5.9)). It should be noted that not the currents and charges calculated by the PEEC-method are used as sources for the field, but the currents and charges calculated by the MoM-method. This is done in order to separate the PEEC-method, used for calculating currents and charges, from the method for calculating the fields.



(a) In the xy-plane. (b) In the yz-plane. (c) In the xz-plane.

Figure 5.28: Normalized far field of the Yagi-antenna.

5.7 Fields of a dipole antenna

5.7.1 Geometry of the dipole antenna

The dipole antenna has a total length of $l = 1$ m, is modelled by copper bars with a square cross-section with a side of $w = 1$ mm and has a gap for attaching a voltage source in the middle with a length of $\delta = 0.01l$ (Fig. 5.29). The xy-coordinate system has its origin in the centre of the gap and the y-axis is aligned with the axis of the antenna. The number of inductive PEEC-segments of the antenna is 84.

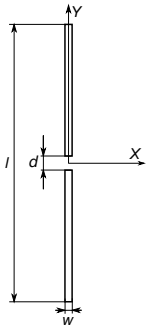


Figure 5.29: Topology of a dipole antenna.

5.7.2 Input admittance of the dipole antenna

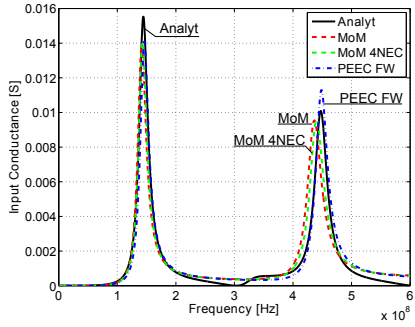
In order to determine the resonance frequency, the input admittance of the antenna is simulated with the full-wave PEEC-method of this thesis, with the Moment Method of [Zwys 12] and with the Moment Method of the freeware antenna analysis tool 4NEC [4nec] (Fig. 5.30a and 5.30b). Also, the theoretical input admittance Y_{theor} of a cylindrical antenna is shown, given by formula (27) of [McDo 09]:

$$Y_{theor} = \frac{1}{Z_{theor}} \quad \text{and} \quad Z_{theor} = \frac{Z_0 k^2 h^2}{2\pi} - j\frac{Z_0}{\pi h k}\ln\left(\frac{h}{a}\right) \tag{5.22}$$

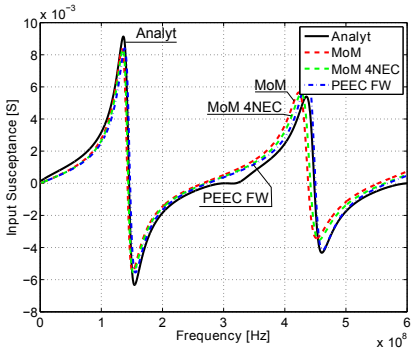
where $Z_0 = \sqrt{\mu_0/\epsilon_0}$, $h = l/2$, $k = 2\pi/\lambda$ and a is the radius of the cylinder. We take $a = \sqrt{w^2/\pi}$. It can be seen from Figs. 5.30a and 5.30b that both the conductance and the susceptance agree well for the four cases. However, there is a small difference in resonance frequencies (i.e. the frequency where the susceptance becomes zero) and conductance at this frequency (Table 5.3).

Table 5.3: First and second resonance frequencies and conductances at these frequencies.

	f_{r1} [MHz]	f_{r2} [MHz]	G at f_{r1} [mS]	G at f_{r2} [mS]
Theoretic	145.4	448.2	15.25	10.06
MoM	142.8	438.2	13.81	9.4
PEEC	147.2	450.1	13.9	11.17



(a) Input conductance of the dipole antenna in function of the frequency.



(b) Input susceptance of the dipole antenna in function of the frequency.

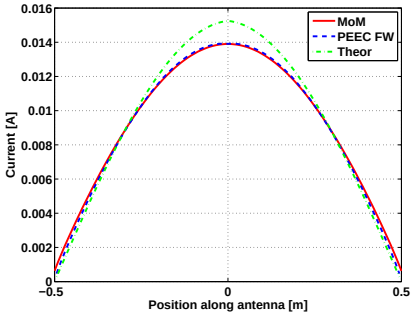
Figure 5.30: Input admittance of the dipole antenna in function of the frequency.

5.7.3 Currents along the axis of the dipole antenna

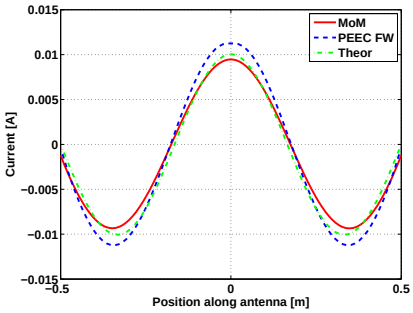
The magnitudes of the currents along the antenna axis at the resonance frequency, which is different for the PEEC-method, the MoM-technique and the theoretical case, are shown in Figs. 5.31a and 5.31b. The theoretical current along the y-axis, is given by [Orfa 14], ch. 22:

$$i(y) = \frac{I_0}{\sin(hk)} \sin\left(k(h - |y|)\right) \tag{5.23}$$

where $h = l/2$, $k = 2\pi/\lambda$ and I_0 is the source current ($I_0 = GV_0$, at resonance, with G the input conductance). A small difference between the three cases can be observed, due to a different input conductance at the resonance frequencies. Suppose that instead of exciting the antenna at resonance frequency, the excitation frequency is exactly equal to 150 MHz. The magnitude of the currents along the antenna axis is then shown in Fig. 5.32 for the three cases. As can be seen, a bigger discrepancy is observed, mainly due to the steep curve of the input susceptance of the antenna around the resonance point. Therefore, it can be concluded that if we want to compare the theoretical (near) field of the antenna with the field calculated by the numerical method of this thesis, it is best to calculate the theoretical field at the resonance frequency, predicted by the theory and to calculate the numerical field at the resonance frequency, given by the numerical method.



(a) Magnitude of the currents along the axis of the dipole antenna at the first resonance frequency.



(b) Magnitude of the currents along the axis of the dipole antenna at three times the first resonance frequency.

Figure 5.31: Currents along the axis of the dipole antenna at a multiple of the first resonance frequency.

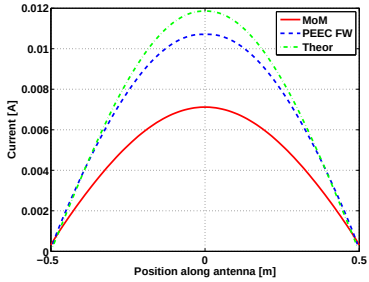


Figure 5.32: Magnitude of the currents along the axis of the dipole antenna at 150 MHz.

5.7.4 Fields of the dipole antenna

Again, as was the case in the two-wire problem and the problem of the Yagi-antenna, we apply the method of this thesis in order to determine the electromagnetic fields:

1. Simulate the PEEC model of the dipole antenna in Spice, using an AC-simulation.
2. Extract from Spice the currents through each inductive cell and the voltages on each capacitive cell, with respect to the node '0', i.e. the space at infinite distance from the model. These currents and voltages are phasors, consisting of an amplitude and a phase.
3. Calculate the charges on each capacitive cell by multiplying the voltage vector with the short-circuit capacitance matrix $[C_s]$, calculated by FastCap, as in eq. (4.9).
4. Modify the node potentials by subtracting a constant K from them:

$$[V'] = [V] - K\,[1 \quad 1 \quad \cdots \quad 1]^T \tag{5.24}$$

where K is given by:

$$K = \frac{\sum_i Q_i}{\sum_i \sum_j C_{s,i,j}} \tag{5.25}$$

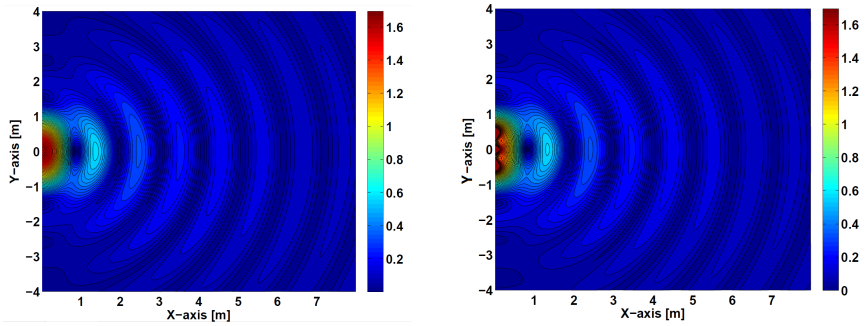
Then, calculate the modified charge vector:

$$[Q'] = [C_s][V'] \tag{5.26}$$

The sum of all charges Q'_i on the capacitive elements is zero:

$$\sum_i Q'_i = 0 \tag{5.27}$$

The derivation of K is given in Section 5.4.4.



(a) Magnitude of the theoretical electric field at time $t = 0$ at the theoretical resonance frequency.

(b) Magnitude of the simulated electric field at time $t = 0$ at the simulated resonance frequency.

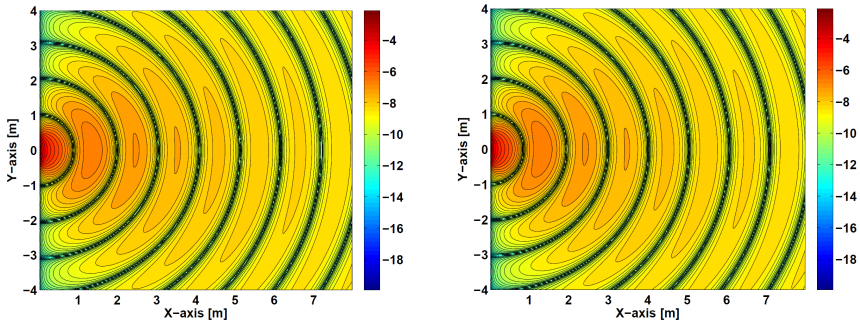
Figure 5.33: Magnitude of the electric field at time $t = 0$ at the resonance frequency.

5. Use the currents and the modified charges to calculate the electric field and the magnetic induction with the frequency-domain equations (5.8) and (5.9).

The theoretical and simulated electric and magnetic fields, together with their contour lines, at time $t = 0$ (the antenna is excited with a cosine voltage source with amplitude 1) are shown in Figs. 5.33a, 5.33b, 5.34a and 5.34b and the normalized far field in the xy-plane is depicted in Fig. 5.35. A very good agreement is observed, hence validating the method of this thesis also for near fields, in the frequency domain. The theoretical near fields are given in ([Orfa 14], p. 1045-1046). The theoretical normalized far field is given by ([Orfa 14], p. 780, formula (17.3.3)):

$$\frac{|\vec{E}|}{E_{max}} = C\sqrt{\left(\frac{\cos(kh\cos\theta) - \cos(kh)}{\sin(\theta)}\right)^2} \tag{5.28}$$

where C is a normalization constant, that is so that the maximum of $|\vec{E}|/E_{max}$ is 1 and θ is 90° minus the elevation angle. As a last check, the radiated power is calculated as the surface integral of the normal component of the Poynting vector over a large sphere (radius = 20 m). The theoretical radiated power is $VI/2 = 1 \cdot 15.25 \cdot 10^{-3}/2 = 0.0076125$ W and the simulated power is 0.0074401891 W. The error between the two is only 2.264 %.



(a) Base-10 logarithm of the magnitude of the theoretical magnetic field at time $t = 0$ at the theoretical resonance frequency.

(b) Base-10 logarithm of the magnitude of the simulated magnetic field at time $t = 0$ at the simulated resonance frequency.

Figure 5.34: Base-10 logarithm of the magnitude of the magnetic field at time $t = 0$ at the resonance frequency.

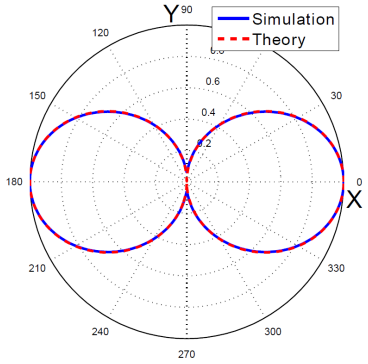


Figure 5.35: Normalized magnitude of the far electric field of the dipole antenna.

5.8 Fields of a theoretical buck converter

In the doctoral thesis of Bruno Bolsens [Bols 05] the fields, currents and voltages of a theoretical buck converter were calculated with the Method of Moments. A superposition technique was used where the switch was replaced by a current source of 1 A and the diode by an open circuit (in practice: a high-ohmic resistor) in the interval $[0, \delta T]$. In the interval $]\delta T, \mathrm{T}[$, the diode is a current source of 1 A and the switch is an open circuit. Here, δ is the duty ratio and T is the period. The frequency components of the current through and the voltage across the switch and diode are calculated with a set of equations expressing that in interval $[0, \delta T]$ the voltage across the switch is zero and the current

through the diode is zero, and that in interval $]\delta T, T[$, the current through the switch and the voltage across the diode are zero. Other equations that make the set of equations solvable express the component equations, $V_x = z_{xx}I_x + z_{xy}I_y$. Here, V_x and I_x are the k^{th} frequency component of the voltage across and the current through element x (x can be the diode or the switch), z_{xx} is the self-impedance of element x and z_{xy} the mutual impedance between x and y. Then, the two states are superimposed and one finally obtains the total currents in every segment of the converter in the frequency-domain. An inverse Fourier transform subsequently gives the time-domain waveforms.

It is deemed useful to test the method of calculating the electromagnetic fields on this switched-mode power supply in order to validate the method further.

5.8.1 Geometry and PEEC-simulation of the buck topology

The topology of the buck converter is shown in Fig. 5.36. The diode D and switch S are ideal and switch at 20 kHz, with a duty cycle of $\delta = 85$ %. The coil has an inductance of $L = 9$ mH and the resistor has a resistance of $R = 100\ \Omega$. The DC voltage source has a value of $V_{DC} = 10$ V. In Bolsens's doctoral thesis the elements are connected with a cylindrical wire with a radius of 1 mm. Because the PEEC-software developed in this work only allows wires with a rectangular cross-section, the cylinders are modelled as bars with a square cross-section with side $w = \sqrt{\pi(1 \cdot 10^{-3})^2}$ m. The bars are copper, and the nodes between the bars or at their endpoints are given in Table 5.4. There is no dielectric substrate; the structure is suspended in air. The size of the panels in the capacitive subdivisions is equal to w. The frequency at which the skin-effect is taken into account is 50 times the switching frequency, 50×20 kHz=1 MHz. Bolsens used segments of 1 cm long, and in this work, the number of inductive segments between two nodes is given in Table 5.5. The PCBParC-software, operated in full-wave mode, extracts a PEEC-model for the copper tracks. This is connected in PSpice with the circuit elements R, L, V_{DC}, S and D and PSpice calculates the currents through all inductive elements and the potential on all capacitive elements (Fig. 5.37).

Table 5.4: Positions of the nodes in the geometry of Fig. 5.36.

Node	x, y coord. [mm]	Node	x, y coord. [mm]	Node	x, y coord. [mm]	Node	x, y coord. [mm]
$N1$	0, -35	$N5$	40, 35	$N9$	100, -5	$N13$	150, -5
$N2$	0, -5	$N6$	50, 35	$N10$	100, -35	$N14$	150, 5
$N3$	0, 5	$N7$	100, 35	$N11$	150, -35	$N15$	150, 15
$N4$	0, 35	$N8$	100, 5	$N12$	150, -15	$N16$	150, 35

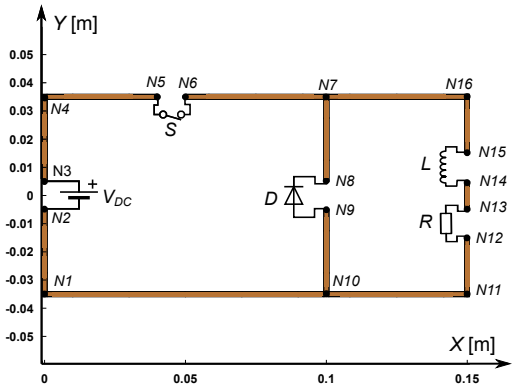


Figure 5.36: Geometry of the buck converter described in the doctoral thesis of Bolsens [Bols 05].

Table 5.5: Number of inductive segments between two nodes in Fig. 5.36.

Segment	Number of subsegments	Segment	Number of subsegments	Segment	Number of subsegments
$N1, N2$	2	$N7, N8$	2	$N13, N14$	1
$N3, N4$	2	$N9, N10$	2	$N11, N12$	2
$N4, N5$	2	$N7, N16$	3	$N10, N11$	3
$N6, N7$	3	$N15, N16$	2	$N1, N10$	5

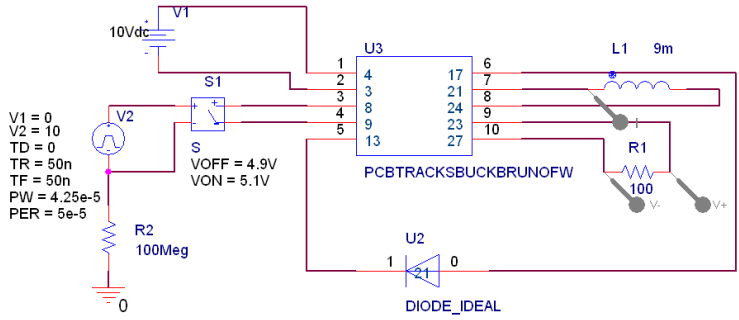


Figure 5.37: Simulating the PEEC-model of the buck described in the doctoral thesis of Bolsens [Bols 05] in PSpice.

5.8.2 Fields around the buck converter

The electric field, magnetic induction and Poynting vector are calculated in a plane parallel to the xy-plane, defined by $z = 1.5$ mm. The $z = 0$-plane cuts through the middle of the copper tracks. The component of the electric

field $\vec{E}$ which is tangential to this plane, is calculated, together with all the (x, y, z)-components of the magnetic induction $\vec{B}$ and the Poynting vector $\vec{S}$. This is done in the frequency-domain, at frequencies 0 and 460 kHz (DC and the 23^{rd} harmonic of the switching frequency), and in the time-domain at instants $t = 548$ μs and $t = 575$ μs, corresponding to two instants, in steady state operation, when the switch of the buck is respectively open and closed.

The same procedure as before is used for calculating the fields: the charges on each capacitive cell are obtained by multiplying the voltages, returned by the Spice-simulation, with the short-circuit capacitance matrix $[C_s]$, calculated by FastCap, as in eq. 4.9. Next, the charges are modified by subtracting a constant K from the voltage vector, given by equation (5.18). Finally, the currents and charges are used to calculate the electric field and the magnetic induction with Jefimenko's equations (5.1) and (5.2) or with the frequency-domain equations (5.8) and (5.9).

The frequency components of the fields are shown in Figs. 5.38a-5.38f, the time-domain fields in Figs. 5.39a-5.39f. For the vectors in the frequency-domain, the Euclidian norm of the amplitudes of the $\vec{E}$- and $\vec{B}$-vector is depicted; in the frequency-domain, this is equal to $\sqrt{2}$ times the RMS-value of the field. For the $\vec{S}$-vector in the frequency-domain and for the $\vec{E}$-, $\vec{B}$- and $\vec{S}$-vector in the time-domain, the real parts are depicted.

Let us first discuss the frequency-domain Figures (Figs. 5.38a-5.38f). The tangential electric field is negligible in the vicinity of the wires. This is because the wires are made from copper and have a very good conductivity. Perfect conductors have only a normal component of the electric field and no tangential component. The line integral of the DC-component of the electric field is calculated over the gap where the voltage source is present, and a value of 9.7 V is obtained, corresponding quite well with the theoretical value of 10 V. The difference with this last value is due to a rather coarse grid (250x200 points), used to calculate the fields on. Some line integrals are calculated to verify the quantitative accuracy of the method. Over the gap of the diode, the line integral of the DC component of $\vec{E}$ is calculated and 8.6 V is obtained, not very different from the theoretical value of 8.5 V. Over the gap where the inductor is present, the line integral of the DC electric field gives 0.07 V, corresponding well with the theoretical value of 0 V. For an AC-component, Fig. (b) shows that across the voltage source and the resistor, only a very small field is present. Across the inductor, on the other hand, a higher voltage is present. This corresponds well with what is theoretically expected. Also the simulation results of the frequency components of the magnetic induction $\vec{B}$, presented in Figs. (c) and (d), show plausible results. In Fig. (c), the DC-component of $\vec{B}$, the current is for 85 % of the time present in the left loop, flows for 15 % of the time through the diode, and for 100 % of the time through the inductor and resistor, thus explaining the differences in colour intensity. In Fig. (d), the inductor blocks high frequency

current, and these current components are therefore only present in the loop constituted by the voltage source, switch and diode.

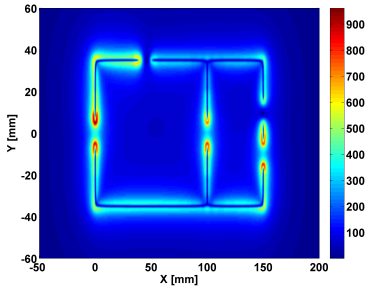
The fieldlines of the DC-component of the Poynting vector and of its 23rd harmonic are shown in Figs. 5.40a and 5.40b. We come to the same conclusion as Bolsens [Bols 05], namely, that there is a high-frequency (HF) channel between the switch and diode. DC-power flows from the voltage source to the switch, which converts it into HF-power. This power travels through space towards the diode, which rectifies it and makes DC-power of it. The DC-power travels further from the diode to the resistor. There is thus a HF-channel present between switch and diode, depicted in Fig. (b). But it can also be seen that some of the HF-power travels from switch to inductor and from there to the diode.

However, when the real part of the normal component of the 23rd harmonic of the Poynting vector on a sphere with radius 100 m is plotted, we do not obtain the results Bolsens described in his work. He obtained both a positive and negative flux on different parts of the sphere, thus indicating that a distance of 100 m is not the far field zone yet. However, in this work, only an outgoing flux is obtained. For a sphere with a radius of 10 m, the flux assumes both polarities though (Fig. 5.41b). The integral of the real part of the normal component of the 23rd harmonic of the Poynting vector over a sphere with radius 200 m is:

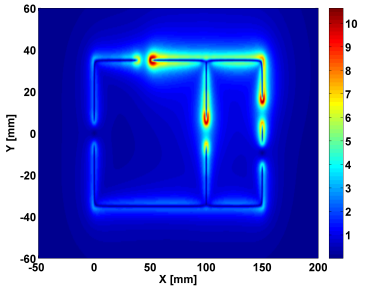
$$\int_{\text{r=200 m}} \text{Re}\left(\vec{S_{23}}\right) \cdot d\vec{A} = 4.795 \cdot 10^{-13} \text{ W} \tag{5.29}$$

This does not correspond at all with Bolsens's result of $3.1982 \cdot 10^{-17}$ W [1]. However, roughly seen, the scale of Fig. 5.41a has an upper limit of about $5.5 \cdot 10^{-18}$, whereas the scale of Fig. 5.41b has an upper limit of $4 \cdot 10^{-16}$. This can be well explained by noticing that far fields decay in strength inversely proportional to the square of the distance. So, if the distance decreases with a factor of 10, the field strength increases with a factor of 100.

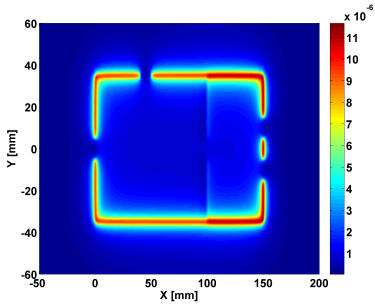
[1] In fact, in Bolsens's doctoral thesis, in formula (3.18), a value of $3.1565 \cdot 10^{-16}$ W is given, but there is in fact an error of a factor of π^2 because in his software code, a mistake was made by equating $\vec{H}$ to $\frac{\vec{B}}{4 \cdot 10^{-7}} \pi$



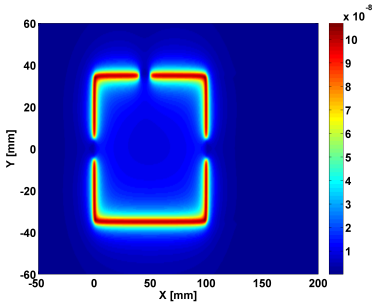
(a) Tangential component of the DC-component of the electric field in the $z = 1.5$ mm plane above the theoretical buck converter (V/m).



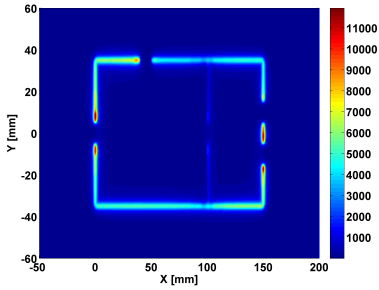
(b) Tangential component of the 23rd harmonic of the electric field in the $z = 1.5$ mm plane above the theoretical buck converter (V/m).



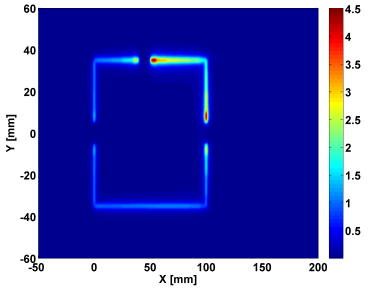
(c) DC-component of the norm of the magnetic induction in the $z = 1.5$ mm plane above the theoretical buck converter (T).



(d) 23rd harmonic of the norm of the magnetic induction in the $z = 1.5$ mm plane above the theoretical buck converter (T).

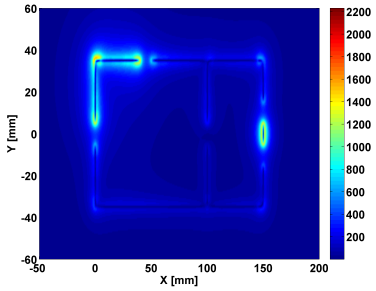


(e) DC-component of the norm of the Poynting vector in the $z = 1.5$ mm plane above the theoretical buck converter (W/m^2).

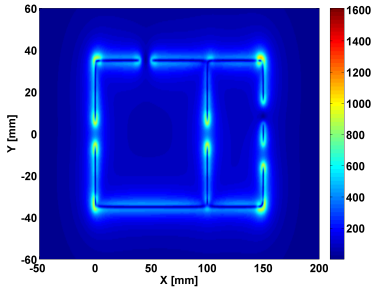


(f) 23rd harmonic of the norm of the Poynting vector in the $z = 1.5$ mm plane above the theoretical buck converter (W/m^2).

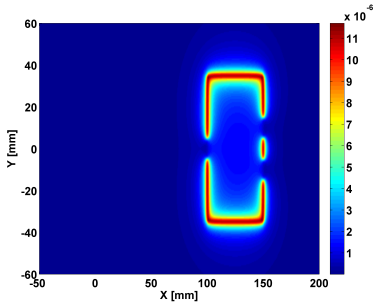
Figure 5.38: Frequency components of the electromagnetic fields in the $z = 1.5$ mm plane above the theoretical buck converter.



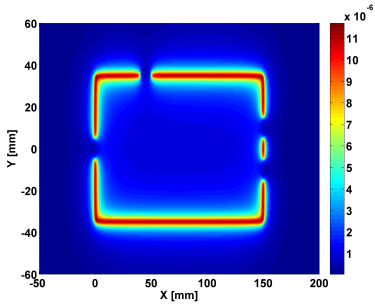
(a) Tangential component of the electric field in the $z = 1.5$ mm plane above the theoretical buck converter when the switch is open (V/m).



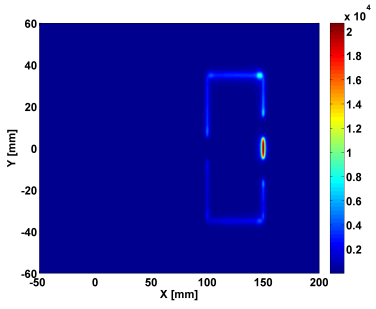
(b) Tangential component of the electric field in the $z = 1.5$ mm plane above the theoretical buck converter when the switch is closed (V/m).



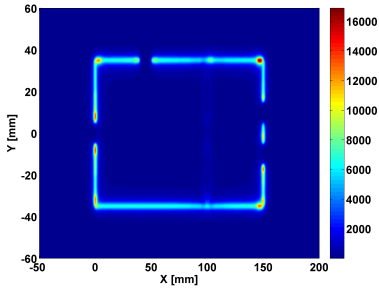
(c) Norm of the magnetic induction in the $z = 1.5$ mm plane above the theoretical buck converter when the switch is open (T).



(d) Norm of the magnetic induction in the $z = 1.5$ mm plane above the theoretical buck converter when the switch is closed (T).

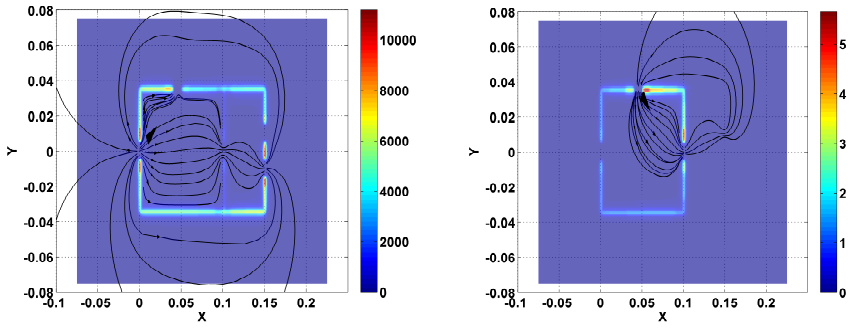


(e) Norm of the Poynting vector in the $z = 1.5$ mm plane above the theoretical buck converter when the switch is open (W/m^2).



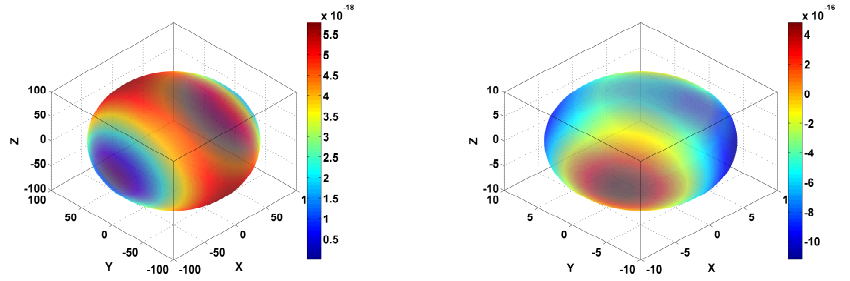
(f) Norm of the Poynting vector in the $z = 1.5$ mm plane above the theoretical buck converter when the switch is closed (W/m^2).

Figure 5.39: Time-domain electromagnetic fields in the $z = 1.5$ mm plane above the theoretical buck converter.



(a) DC component. (b) 23rd harmonic.

Figure 5.40: Fieldline plot of the real part of the DC-component and of the 23rd harmonic of the norm of the Poynting vector (W/m^2) in the $z = 1.5$ mm plane.



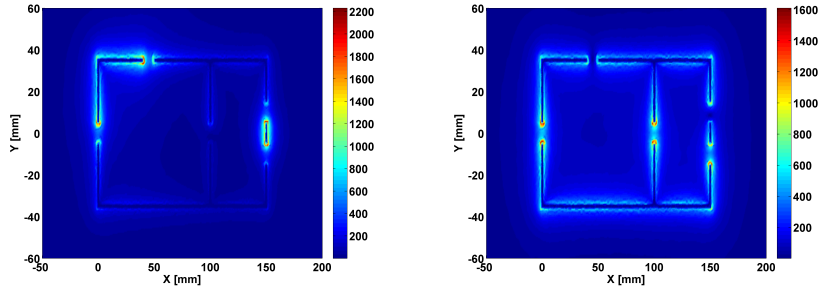
(a) Sphere with radius 100 m. (b) Sphere with radius 10 m.

Figure 5.41: Intensity plot of the real part of the normal component of the 23rd harmonic of the Poynting vector (W/m^2) on spheres with different radii.

5.8.3 Validation of the calculated near electric field

The near electric field obtained in previous Section is compared with the one, obtained from a finite element simulation. Instead of comparing with near field measurements, it was deemed sufficient to compare the results of this work with the field calculated by Comsol [Coms]. Comparisons with measurements were not done because the fields generated by the supply lines leading from the power supply to the circuit, cannot be neglected and they would influence the measurements to a great extent. For this reason, the comparison is done between the results of two different simulation methods, the PEEC method and the finite element method.

Fig. 5.42 shows the tangential component of the electric field in the $z = 1.5$ mm-plane above the buck converter circuit. It is to be compared with the results from the PEEC-simulation, shown in Fig. 5.39. For this purpose, vertical slices, for fixed x-coordinates, are made. Multiple slices were examined, of which two are depicted in Fig. 5.43. As can be seen, a good agreement is reached between the PEEC-simulation and the Comsol finite element simulation. The PEEC-simulation however shows increased electric field values at the 90-degrees-bends of the circuit. However, the volumetric charge distribution is assumed to be uniform in the PEEC-method and thus cannot explain the higher field at the 90-degrees-bend. One can for instance argument that the electric field is higher when the curvature of the metal conductor is higher. However, this would require that the charge density is also higher at the conductor's edges with an increased curvature, which is not the case in the PEEC-method of this work. Except for the vicinity of those 90-degree-bends in the circuit, the correspondence between the results of Comsol and of the PEEC-method is very good.



(a) The switch is open.

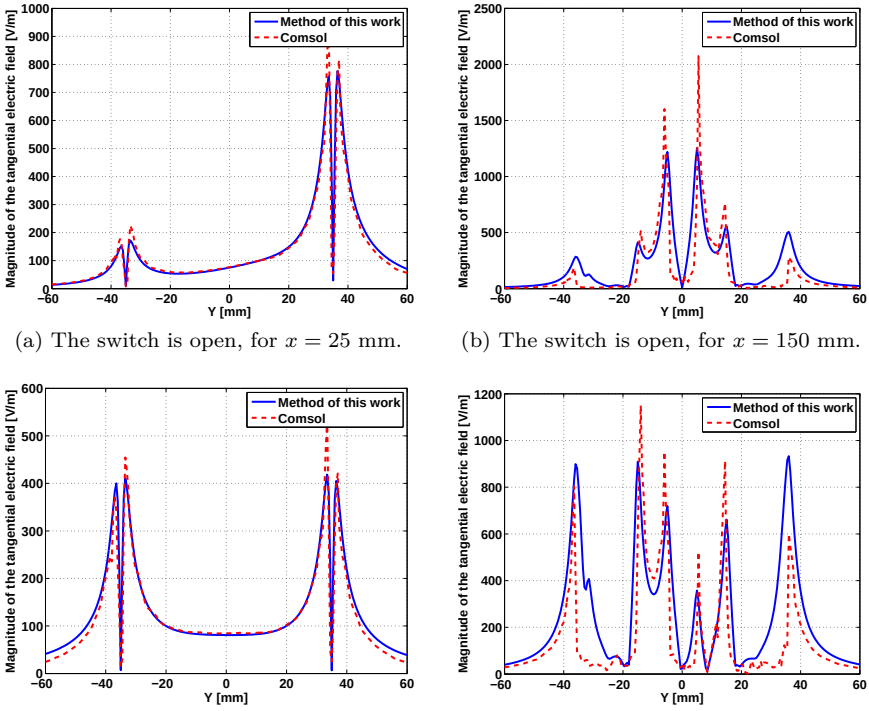
(b) The switch is closed.

Figure 5.42: Comsol simulation of the tangential component of the electric field in the $z = 1.5$ mm plane above the theoretical buck converter (V/m).

It is not necessary to compare the magnetic induction around the buck converter with Comsol-simulations, because in Section 5.5, it was already found that the method and implementation of this work can calculate the transient magnetic induction well.

The difference in calculation speed is remarkable. On a 64 bit machine with 5.87 GB usable RAM and an Intel Quad CPU Q9550 with 2.83 GHz clock speed, the Comsol simulation of the electric field alone (60948 degrees of freedom, from 0 till 0.65 ms with a maximum step size of 100 ns) lasts 14 hours, 7 minutes and 1 second. These are 50821 seconds. The method of this work takes:

1. 77 seconds to run FastHenry, FastCap, produce the Spice-file and save the geometry.



(a) The switch is open, for $x = 25$ mm.

(b) The switch is open, for $x = 150$ mm.

(c) The switch is closed, for $x = 25$ mm.

(d) The switch is closed, for $x = 150$ mm.

Figure 5.43: Comparison of the PEEC and Comsol simulation of the tangential component of the electric field in the $z = 1.5$ mm plane above the theoretical buck converter (V/m).

2. 88 seconds in order to do the PSpice-simulation from 0 till 0.65 ms with a maximum step size of 100 ns.

3. 1505 seconds in order to calculate 10000 harmonics of the currents and voltages.

4. 8809 seconds in order to calculate the electric, magnetic and Poynting fields on a 501x241-point grid.

This results in 10479 seconds.

5.9 Fields of a real reversed buck convertor

5.9.1 EMC testing

The method of this Chapter is next applied to the reversed buck converter of Chapter 4 in order to show a practical application of the method. The geometry is meshed in 34 inductive and 43 capacitive cells and a full-wave simulation is performed.

In order to be able to attribute the CE-mark to an electrical product, which makes it legal to sell it in the European Economic Area, the requirements of the EMC (Electromagnetic Compatibility) Directive 89/336/EEC (published December 31, 2004, took effect on July 20, 2007) have to be satisfied. There are several EMC standards in the Directive, but the most important one is the European Norm EN 55022:2010, which took effect on December 1, 2013. This is essentially the CISPR 22:2008 standard, published by the International Special Committee on Radio Interference (CISPR) which is a committee of the International Electrotechnical Committee (IEC).

CISPR 22:2008 regards the emissions radiated by electrical information technology equipment (ITE). These appliances are subdivided in several categories, and digital devices into the classes A and B. Class A devices are digital devices that are marketed for use in commercial, industrial or business environments. Class B devices are digital devices marketed for use in residential environments. The requirements posed to class B devices are more stringent than those posed to class A devices, because it is assumed that interference from devices in an industrial environment can be more easily corrected than in a residential environment, as industries have the means and knowledge to do these corrections, and interfering devices are more probably located farther apart.

Radiated electric field emissions according to the CISPR 22 standard are to be measured either at an open-area test site (OATS) or in a semianechoic chamber (Fig. 5.44). This a a shielded chamber, having radio-frequency absorbers on its walls and at the top of the room, in order to emulate free space. Only reflections on the bottom floor are possible, for frequencies smaller than 1 GHz. For frequencies higher than 1 GHz, also on the ground, electromagnetic absorbing material is placed. The measurement receiver is a quasi-peak detector for frequencies below 1 GHz. For frequencies from 1 GHz to 6 GHz, the receiver is operated in both average mode and in peak mode. The product is placed at a height of 1 metre and the electric field is measured with antennas at a distance of 10 metres or 3 metres, for frequencies lower than, or respectively higher than 1 GHz. The antenna scans the environment from a height of 1 m above the floor, till a height of 4 metres and the maximum level is recorded. The antenna is

placed in both horizontal and vertical polarization and the maximum recorded emissions in both polarizations is recorded.

The limits on the radiated emissions are shown in Table 5.6 [Info 08]. There is no requirement in CISPR 22 on radiated emissions above 6 GHz, but this will likely change because personal computers already have clock rates in the GHz range, and some work is in progress to extend the frequency range for class B devices to 18 GHz.

Table 5.6: Radiated emission limits for class A and B digital ITE equipment.

	Class A		Class B	
Frequency [MHz]	μV/m	dBμV/m	μV/m	dBμV/m
30-230	100	40	31.6	30
230-1000	224	47	70.8	37
1000-3000	631 (Avg.), 6310 (Pk.)	56 (Avg.), 76 (Pk.)	316 (Avg.), 3162 (Pk.)	50 (Avg.), 70 (Pk.)
3000-6000	1000 (Avg.), 10000 (Pk.)	60 (Avg.), 80 (Pk.)	501 (Avg.), 5012 (Pk.)	54 (Avg.), 74 (Pk.)

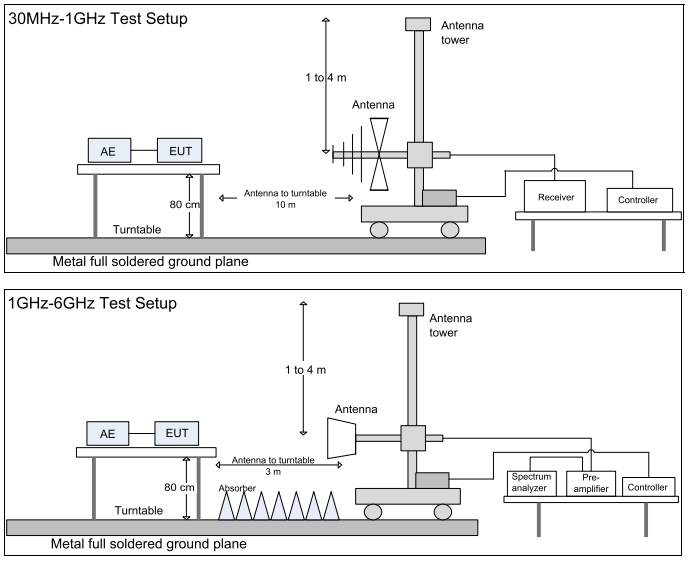


Figure 5.44: Test setup for measurement of radiated emissions according to CISPR 22. EUT=Equipment Under Test, AE = Auxiliary Equipment, Source: International Standards Laboratory [Labo].

The method of this Chapter can be applied to predict the emissions radiated by an electronic device, for instance in the band from 30 MHz to 1 GHz. The

maximum x-, y- and z-components of the electric field at 10 metres distance, where the maximum is recorded from a height of 1 metre till 4 metres, as previously explained, is shown in Fig. 5.45. No groundplane is however taken into account. The measurements are done in a plane parallel to the xy-plane. It can be seen that the reversed buck converter of Chapter 4 does not satisfy the CISPR 22 standards for radiated emissions. The resonance peaks at 36 and 72 MHz are clearly present in the radiated fields.

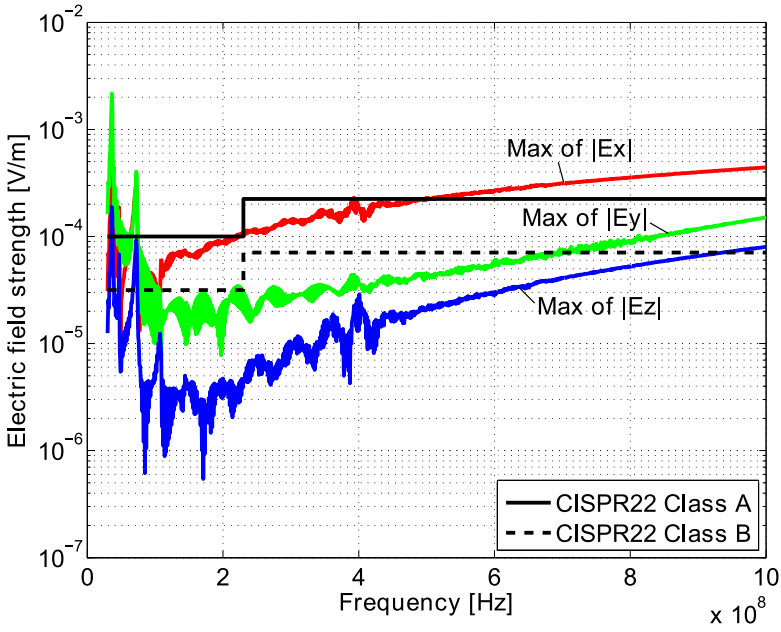


Figure 5.45: Maximum radiated electric field, for frequencies below 1 GHz, at 10 metre distance and the allowed levels according to CISPR 22.

This shows how the method of this work to calculate electromagnetic fields can be applied to predict the radiated emissions and compare them with the allowed limits according to CISPR 22. Similarly, conducted emissions can accurately be predicted with the methods of this work. A Line Impedance Stabilization Network (LISN) has to be inserted then between the AC-grid and the device, and this can easily be simulated in Spice. However, the conducted emissions were not calculated with the method of this work for the reversed buck converter, as it has an input of 40 V DC and is not intended to be directly connected to the power grid.

5.10 Conclusion

This work investigates the opportunities, design and challenges when fast switching frequencies and waveforms with steep flanks are employed in power electronic converters. With very high frequencies, the size of the PCB-loops and tracks become of the same order as the wavelength and converter structures become effective antennas, radiating electromagnetic waves. This Chapter quantifies these fields. This is important so that the emission levels of a converter can be estimated, so that a converter manufacturer knows whether their product fulfils the requirements posed by the emission standards. Furthermore, when the emission mechanism of electromagnetic waves is well investigated and when it is modelled, then the location in the converter where the fields are strongest can be determined and the origin of the production of emissions can be found. This also facilitates the development of techniques to mitigate the production of waves. Finally, another reason why calculating the fields around a converter is important, is that converters almost never stand alone. They are often present in an environment with other electronic devices which can be disturbed by the fields, emitted by the power converters. The signals in power converters have quite low frequencies, as compared to the electronics in information technology equipment, but the powers and energies are much larger. Therefore, they can influence the operation of other electronics in their vicinity to a great extent.

This Chapter calculates the fields around power converters, or in general, around any structure consisting of wires with a rectangular cross-section. The techniques of Chapter 4 are employed to calculate the current and potential distribution on the PCB-tracks. The charges are calculated by multiplying the short-circuit capacitance matrix with the vector of the potentials, on which first a gauge is applied. Currents and charges are the sources of the electromagnetic fields. In the time-domain, Jefimenko's equations are used to determine the fields, but also for the frequency-domain, there exist relationships between the charges and currents on the one side and the fields on the other.

In order to validate the method, it is applied to several cases for which analytical or numerical solutions exist. In order to fairly validate the method of this work, these numerical solutions have to be obtained by the application of other field calculation methods. First, the static fields between two parallel current-carrying wires are calculated analytically, by solving the Laplace equation with the method of separation of variables and bipolar coordinates. These results are used as a benchmark to test the technique of calculating the static fields. The numerical results agree very well with the analytical. Also, the power flow along these lines is visualized giving insight in the propagation of energy throughout transmission line structures.

Next, it is also tested whether non-static fields can be well simulated. The magnetic induction around an RC-circuit is calculated, and the values are

compared with the results produced by the finite element solver Comsol.

Also, a Yagi-antenna structure and a dipole antenna are used to this end. Closed-form expressions for the fields or input impedance exist for these antennas, but also a comparison is made with the results produced by the Method of Moments. Also an earlier step in the field determination process is checked: the calculation of the currents and charges on the wires. Finally, the input impedance is determined in function of the frequency and compared with the analytic value as a validation of the proposed method.

These techniques are then applied to power converters. A buck converter with the same geometry, operating frequency and components as in Bolsens's work [Bols 05] is used. The electric and magnetic fields are determined at two different time instances: when the switch conducts and when the switch is open. Measurements could be done, using near field probes installed on an XY-table, but the author of this work did not opt for this method, because it was expected that the power supply, feeding the converter, and the supply wires, also would generate fields which then would distort the measurement results. The converter is taken alone, detached from the power supply, and is simulated in Comsol. A good agreement between the results of this work and of Comsol is seen, except at the 90-degrees bends of the structure. Also the frequency components are determined and the fieldlines are drawn for the DC-field and for a HF-field. It is verified that DC-power flows from the power source to the switch, which then generates a HF-field flowing to the diode. The diode rectifies this field which after rectification mainly contains a DC-component, and feeds the load. Thus, there is a HF-channel between the switch and the diode, giving rise to power radiation, as Bolsens observed. The radiated power which the converter emits is also calculated but this value does however not correspond with the value Bolsens determined. However, the quasi-static near electric field around the buck converter is well calculated, as a comparison with the results of Comsol shows.

Finally, the fields radiated by the reversed buck converter of Chapter 4 are calculated. It is seen that the method of this work can be applied in order to simulate the conducted and radiated emissions in different frequency bands which can then be compared with their maximum allowed limits; for instance those given by the CISPR 22 EMC standard.

6 Conclusion

6.1 Discussion of and criticism of the research results

6.1.1 Novel fast switching components: wide-bandgap semiconductors

In the **first part** of this work, important characteristics of gallium nitride DHFETs manufactured by Imec were measured, such as the gate charge necessary to turn the transistors on or off and the dynamic on-resistance. These two quantities are combined in Baliga's High-Frequency Figure Of Merit. In order to truly compare different transistor technologies, the gate charge and the dynamic on-resistance must be scaled with the chip area; only 'specific' quantities must be used to determine the figure of merit. However, the chip area is normally not given in a transistor's datasheet, hence it is difficult to obtain the data to perform the scaling. This problem is circumvented in this work by comparing the non-scaled figures of merit of transistors that have approximately equal voltage and current capabilities. While theoretically gallium nitride has a BHFFOM which is 81 times better than silicon (cf. Table 2.3), Imec's devices ranked not good at all as compared to ordinary silicon devices (Fig. 2.27). Possible causes for this can be the chip layout, the purity of the gallium nitride crystal or even the fact that the current collapse phenomenon is not fully resolved in these devices. On the other hand, the commercially available components

manufactured by EPC performed much better and ranked better than the group of the silicon 200 V-transistors. When their FOM (0.098 Ω.nC) is compared with the median FOM (1.4 Ω.nC, IXFR140N20P), it can be easily calculated that the EPC devices are approximately 14 times 'better'.

When the measurements are compared with the PSpice simulation results, it is often seen that both disagree. Temperature effects cannot explain the difference as care was taken that the measurements did not heat up the devices. For instance, the static on-resistance was measured by applying voltage pulses to the gate of the transistor and these were short enough not to heat up the semiconductor junctions. The measurement equipment was correctly calibrated, measurement offsets were taken into account and it is thus concluded that one should be very careful when relying on complex Spice-models for determining macroscopic electrical quantities. These models do not always represent reality well. In many cases they do, but in other, they do not. However, no statistical analysis was performed. Only one device of its kind was measured and these results were compared with the Spice-simulations. Even then, the discrepancies can be so large that it is very difficult to judge with good reason in advance whether Spice-models are in fact appropriate for determining on-resistance and gate charge.

Another important remark is that the measurements of the dynamic on-resistance are the only ones that are performed in conditions where the semiconductor junctions heat up. These measurements are therefore not reliable. A better method to perform them is by applying only a few gate-pulses so that the junction is not heated too much with respect to the ambient environment. In fact, it is better to do all the measurements in the temperature-controlled environment of a climate cabinet, if available. For the modelling of the current collapse mechanism in Spice, one can say that this is not standard yet. The models of Imec and EPC did not model current collapse at all; and since the current collapse in these HEMTs is still present, Spice-models can only be accurate when they take this phenomenon into account. Therefore, the author encourages more research particularly into the current collapse mechanism and the modelling thereof.

A voltage-clamping circuit was designed and built to solve the problem of directly measuring the dynamic on-resistance with an oscilloscope. In that case, the drain-to-source voltage is measured; but in order not to saturate the internal amplifiers of the oscilloscope, the off-state drain-to-source voltage must also be displayed on the screen, thus resulting in very inaccurate measurements for the on-state voltage as the entire voltage range is typically measured with only 8 bits of resolution. The voltage-clamping circuit of this work clamps the off-state voltage to a much lower value and allows for accurate measurements of the dynamic on-resistance. It is patented, because of its novelty and practical applicability. However, there is still a problem if the high-voltage diodes have too

large parasitic capacitances. When the drain potential changes and goes either up or down, the parasitic capacitances try to keep the voltage momentarily constant and this results in spikes in the clamped voltage. If these spikes are too large, this can also decrease the resolution. Therefore, the high-voltage diodes in the clamping circuit must be chosen with care.

6.1.2 Resonant converters

In the **second part** of the text a soft-switching resonant convertor is designed and built. It is the first soft-switched converter, realized in research group Electa. In order to show the strength of this type of converter, very ambitious goals for power and frequency were set, which hard-switching converters using traditional silicon components cannot reach. Namely, the converter should operate with a frequency of at least 2 MHz and deliver at least 50 W. All steps in the design of this converter are discussed in detail in this text, and this is a merit of this work. At the same time, the extensiveness of this discussion shows that resonant converters are quite complex and it is not easy for design engineers to realize them.

Sufficient conditions for zero voltage switching were derived. It was seen that there is both an upper limit and a lower limit for the dead time. The voltage dependency of the output capacitance C_{oss} is hereby of great importance and the analysis is not so straightforward as in hard-switching converters. The choice of MOSFETs is quite critical. If the output capacitor of MOSFETs collects too much charge and if the dead time is too low or the resonant tank draws a too small current, zero-voltage switching cannot be obtained. The switching occurs in that case with losses and the transistors can become too warm and be destroyed.

Apart from the choice of MOSFETs, also the design of the passive components is extremely critical when building converters operating at high frequencies. Capacitors must respond quickly (thus have a low Equivalent Series Inductance (ESL)) and provide enough ripple current. Often, the ESL or in other words, the self-resonating frequency of capacitors, is not specified and this leads to the fact that a designer has to choose another brand or type of capacitors. The ESL can be diminished by parallelling capacitors, but this also increases the footprint of placing these capacitors. Ceramic capacitors are fast but lose their capacitance at high voltages. Hence, film capacitors are often a better choice. However, even for the frequencies of this doctoral work, the current capacitor technology is still sufficient but the technology of the magnetic components faces more problems. It was shown in [Perr 09] that when using a lossy magnetic core, the size of inductors first decreases with frequency but then increases again, because with a decreasing size the core cannot be sufficiently cooled. Therefore, at multi-megahertz frequencies, lossless air-cores become a good choice. It was

shown in this work that the size of an air-core inductor suitable for this work is still acceptable. However, it would be good to perform research, perhaps with magnetic field calculations, to determine whether the magnetic coupling in transformers is adequate when an air-core is used. In this work, it was assumed that the coupling is not enough and for this reason, a transformer was designed with a ferrite core. In this core, a large part of the total converter losses occurs, and therefore the use of ferrite cores must be avoided, if possible. On another note, it is possible that the EMI caused by the converter becomes too much when air-cores are used, thus a ferrite core, conducting the magnetic flux, can have its advantages from this point of view.

Optimal values for the elements in the resonant tank were determined with an iterative analysis. However, as parasitic elements of the transformer were used to serve as the elements of the resonant tank, it is difficult to realize these optimal values. The magnetization inductance, being much greater than the leakage inductance, can be designed to approach the optimal value, but it is much more difficult to design and obtain a desired value for the leakage inductance. In this work, a transformer was first built and afterwards, it was seen that the measured leakage inductance still had an acceptable value, not too different from the optimal value to be detrimental.

To model the converter, a high-frequency transformer model was used. The most important problem with this model is the fact that it does not accurately model hysteresis losses. Therefore, it is not so good to predict efficiency. An improvement to the transformer model can be the modelling of the core losses and can be done from first principles.

A half-bridge gate-driver was developed and constructed. A problem the author sees for high-frequency drivers is that the driver IC cannot deliver enough current anymore at these multi-megahertz frequencies. To give an example, up to 1 MHz, the TC4422 driver IC can be used, supplying 9 A, but for higher frequencies, mainly because of the large crossover constant CC (see Section 3.7) of the driver chip, another IC was selected, TC4427, being able to deliver only 3 A to the MOSFETs. The driver works fine, but it should also be acknowledged that because it works with an XOR-gate, the two signals, high-side and low-side, are complementary. That means that when the signal generator, supplying the control signal to the gate-driver, is turned off, one of the MOSFETs (high-side or low-side, depending on the specific wiring scheme) is kept on while the other is turned off. This can easily be remediated by also using an enable signal and AND-gates, but is of no problem in this work.

The converter was built, and ZVS is observed at light load. However, at a heavy load of 4.5 Ω, ZVS could not be reached. The minimal load resistance for which ZVS was obtained, was 5.65 Ω. The converter has an efficiency of 84.2 % at this load and the gain curves are measured and show a good resemblance with the theoretically predicted, making use of the lumped transformer model.

The resonant current was also integrated over time in order to determine the charge that the output capacitors of the MOSFETs store at the employed supply voltage. This calculation gave a larger value than the value obtained when the datasheet curves of C_{oss} were integrated over the voltage, thereby giving an explanation for the fact that theoretically, it was predicted that ZVS was possible at a load of 4.5 Ω, but that the reality proved to be different.

6.1.3 Modelling PCB-parasitics with the PEEC-method

The **third part** of the work deals with the problem of the prediction of ringing, signal distortion and overvoltages and -currents due to the presence of parasitics in the circuit. First, the author worked for a long time on the Moment Method but he deemed it less flexible than the PEEC-method, outlined in this work. The latter can operate both in the time-domain and in the frequency-domain, but the main advantage is that it extracts an *RLC*-network for the structure of the PCB-tracks which can be imported in a Spice-solver. Then, other elements such as MOSFETs, IGBTs, diodes and also passive components can be inserted and this resulting model can be solved in Spice. The advantage is that pre-existing semiconductor models can be included to accurately simulate the ringing, overshoot, crosstalk and distortion of the signals in a converter. With the Moment Method, operating in the frequency-domain, these models do not exist. However, in Electa, work is being done about building a frequency-domain circuit simulator. Another advantage of the PEEC-method is that one works with the concepts of voltage, current and power, and that one does not have to think in terms of electric and magnetic fields. This makes the design process a lot easier for engineers.

FastHenry and FastCap are used in order to calculate the partial elements. They are freeware software programmes, and are optimized for these calculations, so it was deemed that is was not necessary to write one's own code for this purpose, but instead use FastHenry and FastCap.

The developed PEEC-tool, PCBParC, is freely downloadable. It exists both in a quasi-static version and in a full-wave version, so that also radiation phenomena can be researched and visualized. The quasi-static implementation is very fast, but the full-wave version is actually still too slow to use on complex structures. The generation of the Spice netlist is quick but Spice solves it very slowly, at least for structures that are divided in many segments. It is not only applicable to power electronic circuits but to electronics in general.

The tool was tested extensively, both on linear and nonlinear circuits, and then applied to a reversed buck converter, where long PCB-tracks are used on purpose in order to have large parasitics in the circuit. The gallium nitride HEMT from EPC is used, operating at 1 MHz. The voltage across and the

current through the switch are measured and simulated. The agreement is quite well, except for the current. A possible cause can be that the Spice-model of the EPC-component or of the diode is not accurate enough. However, the most important conclusion is the fact that the exact layout of the PCB-tracks is of great importance for the behaviour of voltages and currents when fast changing (pulse) voltage excitations occur. With faster components, such as the wide-bandgap components or silicon components that require a small gate charge, the waveform's edges become steeper and parasitics become more problematic because steeper pulses excite stronger oscillations.

The work in this part of the text is thus very useful. The method of this work predicts these oscillations, the cross-talk and the signal distortion, but it does not give us guidelines on how to avoid them. This work assumes it is up to the circuit designer to use his or her knowledge about circuit design and come up with a well-designed circuit. Then, it can be checked with the PEEC-method whether the signal integrity and the ringing in the circuit are acceptable. If not, the designer is sent back to the design table and has to apply tricks to modify the circuit in order to solve the signal problems.

The described PEEC-tool only models the PCB-tracks. However, it is shown in literature that the PEEC-method can be applied to a multitude of geometries, also to inductors and capacitors for instance. This work did not model these components electromagnetically, it only models them as lumped *RLC*-circuits. However, the implementation can be extended in order to model the complete circuit with the PEEC-technique; not only the PCB-tracks. This will increase the accuracy of the modelling technique.

6.1.4 Electromagnetic field calculation

The **last part** of the work uses the PEEC-method to calculate currents and potentials on electric structures. The potentials are then converted into charges, by using the short-circuit capacitance matrix. With the currents and charges, the electromagnetic fields around these structures are calculated. This is a full-wave technique, developed in cooperation with Jeroen Zwysen from Electa. The Jefimenko's equations are used to calculate the fields in function of time, and other expressions are developed for calculating the fields in the frequency-domain.

To validate the technique, the method was applied to well-known antenna topologies for which analytical expressions exist and the results of this method agree well with the analytical results.

It was then applied to a theoretical buck convertor, employing an ideal switch and diode. This topology was researched in a previous doctoral work by Bruno Bolsens, but the results of the analysis of this work do not correspond

quantitatively with Bolsens's results. For instance, the 23^{rd} harmonic of the signals on the converter radiates $3.2 \cdot 10^{-17}$ W according to Bolsens, while this work predicts $4.8 \cdot 10^{-13}$ W. However, it is also observed in this work, as was the case in Bolsens's work, that there is a high-frequency channel between the switch and diode. DC-power flows from the voltage source to the switch, which converts it into HF-power. This power travels through space towards the diode, which rectifies it and makes DC-power of it. The DC-power travels further from the diode to the resistor.

In order to further verify the method of this work on switching converters and not only on linear circuits, the electric field of the ideal buck converter is also calculated with a finite element technique (Comsol) and the results are compared with those of this work. It was first considered to perform measurements with near field probes, moved and positioned on an xy-table, but this was expected to give bad results, because the power supply and its leads would also emit fields, distorting the fields of the actual circuit-under-test. The comparison with the Comsol results is very good, except for the vicinity of the 90-degree bends in the circuit.

Finally, the work is applied to calculate the emissions of the reversed buck converter of Chapter 4. The techniques of this work are used to check whether the designed power converter complies with the EMC-regulations for radiated emissions or radiated susceptibility. It makes it possible to avoid having expensive measuring equipment such as antennas, an anechoic chamber, a network analyzer,..., or order tests in a specialized laboratory. The work thus has an immediate practical applicability and is of significant economic value as well. However, according to the CISPR 22 standards for the radiated interference tests, a ground plane is necessary in the test setup for frequencies up to 1 GHz and the developed tool, PCBParC, does not allow to model this conductive plane, in its current form.

6.2 Future work

The author would like to give some advice to future researchers and also some ideas for follow-up work regarding the topics discussed in this Thesis:
Regarding the **transistor characterization** work:

- The FOMs should be accurately scaled in order to obtain results which are independent of the chip area.
- When performing the dynamic on-resistance measurements, pulsed measurements can be used in order to limit the semiconductor heating.

- Preferably, all characterization measurements should be performed in a climate chamber, where the temperature can be controlled.
- Spice-models must be investigated in order to find whether they are suitable for extracting gate charge and on-resistance data.
- The Spice-models of HEMTs must be extended in order to take the current collapse phenomenon into account.
- A method must be devised in order to select the optimal wide-bandgap transistor and diode for a certain application. That is, given the power, voltage and frequency specifications, and a database of transistor and diode data, decide on which transistor and diode are best to choose in order to get the highest efficiency, or the lowest cost, or the smallest size, or even the highest reliability.
- The converters with these optimum diodes and transistors must be built and must be compared with converters built with classical switching components. Size, efficiency, cost or reliability must be investigated.
- The clamped voltage in the voltage-clamping circuit for measuring the dynamic on-resistance can have too large voltage spikes caused by too large parasitic capacitances of the high-voltage diodes. Therefore, it can be studied whether a separate circuit can be developed which quickly charges or discharges these capacitors, in order to mitigate these spikes.

Regarding the work on the **soft-switching resonant converters**:

- It is good to accurately research the benefits and disadvantages of current and upcoming capacitor technologies and magnetic core technologies. Passives will be very critical components in converters of the near future. A separate study must be dedicated to them, especially to magnetic cores. It can be researched up to which frequency and flux density a magnetic core is still useful, or that an air-core is preferential.
- If air-cores will be used for transformers, it must be researched whether the magnetic coupling between the primary and secondary side is still sufficient.
- Also, it is useful to investigate whether the EMI in circuits with air-cores does not lead to a violation of the EMC-regulations.
- When incorporating the parasitics of the transformer in the resonant tank, luck played a too important role. First a transformer was designed and then the value of the leakage inductance was checked. Fortunately, it had an acceptable value, but what happens if the value is too different from the optimal value? A method should be researched to predict the leakage inductance based on the design of the transformer.

- The transformer model should be extended in order to more accurately model the core losses. This can be done based on first principles.

Regarding the work on the **PEEC-modelling technique** and the **field calculations**:

- With the PEEC-technique, an electric circuit should always be segmented in smaller pieces, which are 'much smaller' than the wavelength of the highest occurring frequency. It must be researched what is this frequency when instead of sinusoidal waveforms, there are signals which consist of harmonics. Up to which frequency do we consider the frequency content of the signal? And what is 'much' smaller? It is good to research this in a future work.
- The current version of PCBParC works only for a single-layer PCBs and the PCB-tracks should be straight or have right angles, and be parallel or orthogonal to each other. The code can therefore be extended for other topologies as well, such as PCB-tracks under other angles, multi-layered boards, groundplanes,....
- It can be extended so that it can import PCBs designed in Altium or other tools.
- It can be extended so that it models also the current redistribution due to the skin-effect or the proximity-effect, for instance with the method of Fig. 4.7.
- The full-wave code of PCBParC must be optimized to allow Spice to solve circuits faster.
- The PEEC-software should be used extensively in order to further validate the code.
- Extend the software to also model inductors, capacitors and large film or wire-wound resistors with the PEEC-technique. This is especially necessary to obtain accurate field calculations.

A

Data for Fig. 2.27

Table A.1: Data for comparison of the high-frequency figure of merit of various devices for which either the voltage or current rating are similar to those of the EPC1010-device and Imec's HEMT device.

Device	$\mathbf{V_{DD}}$	$\mathbf{I_{ds}}$ **(continuous)**	$\mathbf{R_{on,stat}}$	$\mathbf{Q_{gd}}$
EPC1010	200V	12A at 25 degrees casing	0.028 Ω at 4.9V V_{gs}	3.5 nC at 100 V, 1.5 A
FDP42AN15A0	150 V	35 A at 25 degrees casing	0.036 Ω at 12 A, 10 V V_{gs}	6.9 nC at 75 V, 12 A, 10 V V_{gs}
FDB2614	200V	62A at 25 degrees casing	0.0229 Ω at 31 A, 10 V V_{gs}	18 nC at 100V, 62A, 10V V_{gs}
IRFB4227PbF	200 V	65 A at 25 degrees casing	0.0197 Ω at 10 V V_{gs}, 46 A	23 nC at 100V, 46A, 10V V_{gs}
IRFP4227PbF	200 V	65 A at 25 degrees casing	0.021 Ω at 46 A, 10 V V_{gs}	23 nC at 100V, 46A, 10V V_{gs}
IRFB4127PbF	200V	76A at 25 degrees casing	0.017 Ω at 44A, 10 V V_{gs}	31 nC at 100V, 44A, 10 V V_{gs}
IRFS4127PbF	200V	72A at 25 degrees casing	0.0186 Ω at 44 A, 10 V V_{gs}	31 nC at 100V, 44A, 10 V V_{gs}
STB75NF20	200V	75A at 25 degrees casing	0.028 Ω at 37 A, 10 V V_{gs}	34 nC at 160 V, 75A, 10 V V_{gs}
SUM65N20-30	200V	65A at 25 degrees casing	0.023 Ω at 30 A, 10 V V_{gs}	34 nC at 100 V, 85A, 10 V V_{gs}
IRFP4768PbF	250V	93 A at 25 degrees casing	0.0145 Ω at 56A, 10 V V_{gs}	72 nC at 125 V, 56 A, 10 V V_{gs}
IRFBA90N20D	200V	98 A at 25 degrees casing	0.023 Ω at 59 A, 10 V V_{gs}	75 nC at 160 V, 59 A, 10 V V_{gs}
STP12NM50	550V	12 A at 25 degrees casing	0.3 Ω at 6 A, 10 V V_{gs}	18 nC at 400 V, 12 A, 10 V V_{gs}
IXFR140N20P	200V	90A at 25 degrees casing	0.014 Ω at 140 A, 15V V_{gs}	100 nC at 100 V, 45 A, 10 V V_{gs}
IRFP4232PbF	250V	60 A at 25 degrees casing	0.030 Ω at 42 A, 10 V V_{gs}	60 nC at 125 V, 42 A, 10 V V_{gs}
IXFN140N20P	200V	115A at 25 degrees casing	0.014 Ω at 140 A, 15V V_{gs}	110 nC at 100 V, 70 A, 10 V V_{gs}
IPA50R299CP	550 V	12 A at 25 degrees casing	0.27 Ω at 6.6 A, 10 V V_{gs}	23 nC at 400 V, 6.6 A, 10 V V_{gs}
IXFH120N20P	200V	120A at 25 degrees casing	0.022 Ω at 65A, 10 V V_{gs}	75 nC at 100 V, 65 A, 10 V V_{gs}
IXTH96N20P	200V	96A at 25 degrees casing	0.024 Ω at 48 A, 10 V V_{gs}	80 nC at 100 V, 48A, 10 V V_{gs}
IXTK100N25P	250V	100 A at 25 degrees casing	0.027 Ω at 50 A, 10 V V_{gs}	91 nC at 125 V, 50A, 10 V V_{gs}
Imec GaN	200V	unknown	0.25 Ω at 0.6155V V_{gs}	8 nC at 100 V, 1.5A
IRFP90N20D	200V	94A at 25 degrees casing	0.023 Ω at 56 A, 10 V V_{gs}	87 nC at 160 V, 56 A, 10 V V_{gs}
IXFN120N20	200V	120A at 25 degrees casing	0.017 Ω at 60A, 10 V V_{gs}	160 nC at 100 V, 60 A, 10 V V_{gs}
IRL3215PbF	150 V	12 A at 25 degrees casing	0.166 Ω at 7.2 A, 10 V V_{gs}	21 nC at 120 V, 7.2 A, 5 V V_{gs}
IXFK90N20	200V	90A at 25 degrees casing	0.023 Ω at 45 A, 10 V V_{gs}	190 nC at 100 V, 45 A, 10 V V_{gs}
IRFP9240	200V	12A at 25 degrees casing	0.5 Ω at 7.2 A, 10 V V_{gs}	27 nC at 160 V, 11 A, 10 V V_{gs}

B

Selection of Core Types and Sizes for the LLC-Converter

Table B.1: Ferroxcube: Planar E core selection - part 1.

Core name	Planar E PLT 14/5/1.5	Planar E PLT 14/5/1.5/S	Planar E PLT 18/10/2/S
P_{core} [W]	2.5	2.5	2.5
P_{cu} [W]	1	1	1
P_V [kW/m^3]	10417	10870	3012
B_{max} [mT]	48.25	49.11	28.77
N_1	21	21	13
N_2	2	2	1
L_1 [uH]	27.783	27.783	16.9
C_r [nF]	0.912	0.912	1.499
d_1 [mm]	0.053	0.053	0.044
d_2 [mm]	0.216	0.216	0.180
$P_{V,max}$ [kW/m^3]	588	608	1280
Core name	Planar E PLT 14/5/1.5	Planar E PLT 14/5/1.5/S	Planar E PLT 18/10/2/S
P_{core} [W]	2	2	2
P_{cu} [W]	0.5	0.5	0.5
P_V [kW/m^3]	8333	8696	2410
B_{max} [mT]	43.97	44.75	26.22
N_1	23	23	14
N_2	2	2	
L_1 [uH]	33.327	33.327	19.6
C_r [nF]	0.760	0.760	1.29
d_1 [mm]	0.076	0.076	0.063
d_2 [mm]	0.311	0.311	0.259
$P_{V,max}$ [kW/m^3]	588.1497	608.4676	1280.384
Core name	Planar E PLT 14/5/1.5	Planar E PLT 14/5/1.5/S	Planar E PLT 18/10/2/S
P_{core} [W]	1.25	1.25	1.25
P_{cu} [W]	1.25	1.25	1.25
P_V [kW/m^3]	5208	5435	1506
B_{max} [mT]	36.15	36.79	21.55
N_1	28	29	17
N_2	3	3	2
L_1 [uH]	49.392	52.983	28.900
C_r [nF]	0.513	0.478	0.876
d_1 [mm]	0.057	0.057	0.051
d_2 [mm]	0.231	0.233	0.210
$P_{V,max}$ [kW/m^3]	588	608	1280

Table B.2: Ferroxcube: Planar E core selection - part 2.

Core name	Planar E PLT 22/16/2.5	Planar E PLT 22/16/2.5/S	Planar E PLT 32/20/3/R	Planar E PLT 38/25/4	Planar E PLT 43/28/4
P_{core} [W]	2.5	2.5	2.5	2.5	2.5
P_{cu} [W]	1	1	1	1	1
P_V [kW/m^3]	1225	1190	548	296	217
B_{max} [mT]	19.78	19.54	14.15	10.94	9.62
N_1	10	9	8	7	7
N_2	1	1	1	1	1
L_1 [uH]	16	12.96	10.24	12.25	12.25
C_r [nF]	1.583	1.954	2.474	2.068	2.068
d_1 [mm]	0.046	0.045	0.054	0.035	0.035
d_2 [mm]	0.187	0.183	0.219	0.142	0.142
$P_{V,max}$ [kW/m^3]	2326	2380	4068	6181	7743
Core name	Planar E PLT 22/16/2.5	Planar E PLT 22/16/2.5/S	Planar E PLT 32/20/3/R	Planar E PLT 38/25/4	Planar E PLT 43/28/4
P_{core} [W]	2	2	2	2	2
P_{cu} [W]	0.5	0.5	0.5	0.5	0.5
P_V [kW/m^3]	980	952	439	236	174
B_{max} [mT]	18.02	17.81	12.89	9.96	8.77
N_1	11	10	9	8	8
N_2	1	1	1	1	1
L_1 [uH]	19.36	16	12.96	16	16
C_r [nF]	1.308	1.583	1.954	1.583	1.583
d_1 [mm]	0.066	0.065	0.077	0.050	0.050
d_2 [mm]	0.269	0.264	0.316	0.206	0.206
$P_{V,max}$ [kW/m^3]	2326	2380	4068	6181	7743
Core name	Planar E PLT 22/16/2.5	Planar E PLT 22/16/2.5/S	Planar E PLT 32/20/3/R	Planar E PLT 38/25/4	Planar E PLT 43/28/4
P_{core} [W]	1.25	1.25	1.25	1.25	1.25
P_{cu} [W]	1.25	1.25	1.25	1.25	1.25
P_V [kW/m^3]	613	595	274	148	109
B_{max} [mT]	14.82	14.64	10.60	8.19	7.21
N_1	13	13	11	9	9
N_2	1	1	1	1	1
L_1 [uH]	27.04	27.04	19.36	20.25	20.25
C_r [nF]	0.937	0.937	1.308	1.251	1.251
d_1 [mm]	0.043	0.043	0.051	0.033	0.033
d_2 [mm]	0.176	0.176	0.207	0.133	0.133
$P_{V,max}$ [kW/m^3]	2327	2380	4069	6182	7743

Table B.3: Ferroxcube: Planar ER, RM8/I and TX13 core selection.

Core name	Planar ER11/2.5/6	Planar ER14.5/3/7	Planar ER18/3/10	RM8/I	TX13/7.5/5
P_{core} [W]	2.5	2.5	2.5	2.5	2.5
P_{cu} [W]	1	1	1	1	1
P_V [kW/m^3]	14368	7508	3748	1025	6793
B_{max} [mT]	55.17	42.10	31.52	18.36	40.38
N_1	23	20	16	13	30
N_2	2	2	1	1	3
L_1 [uH]	33.327	40	332.8	16.9	414
C_r [nF]	0.760	0.633	0.076	1.499	0.061
d_1 [mm]	0.038	0.042	0.036	0.038	0.040
d_2 [mm]	0.154	0.169	0.148	0.156	0.163
$P_{V,max}$ [kW/m^3]	532	799	1244	2909	1508
Core name	Planar ER11/2.5/6	Planar ER14.5/3/7	Planar ER18/3/10	RM8/I	TX13/7.5/5
P_{core} [W]	2	2	2	2	2
P_{cu} [W]	0.5	0.5	0.5	0.5	0.5
P_V [kW/m^3]	11494	6006	2999	820	5435
B_{max} [mT]	50.27	38.36	28.72	16.73	36.79
N_1	25	22	17	14	33
N_2	2	2	2	1	3
L_1 [uH]	39.375	48.4	375.7	19.6	500.94
C_r [nF]	0.643	0.523	0.0674	1.292	0.051
d_1 [mm]	0.054	0.0598	0.063	0.055	0.057
d_2 [mm]	0.222	0.244	0.259	0.224	0.235
$P_{V,max}$ [kW/m^3]	532	799	1244	2909	1508
Core name	Planar ER11/2.5/6	Planar ER14.5/3/7	Planar ER18/3/10	RM8/I	TX13/7.5/5
P_{core} [W]	1.25	1.25	1.25	1.25	1.25
P_{cu} [W]	1.25	1.25	1.25	1.25	1.25
P_V [kW/m^3]	7184	3754	1874	512	3397
B_{max} [mT]	41.33	31.54	23.61	13.75	30.25
N_1	30	27	21	17	40
N_2	3	2	2	2	4
L_1 [uH]	56.7	72.9	573.3	28.9	736
C_r [nF]	0.447	0.347	0.044	0.876	0.034
d_1 [mm]	0.040	0.039	0.042	0.044	0.041
d_2 [mm]	0.164	0.161	0.170	0.182	0.168
$P_{V,max}$ [kW/m^3]	532	799	1244	2909	1508

Table B.4: Ferroxcube: EQ core selection.

Core name	EQ13	EQ20/R	EQ25	EQ30
P_{core} [W]	2.5	2.5	2.5	2.5
P_{cu} [W]	1	1	1	1
P_V [kW/m^3]	71834	1276	603	503
B_{max} [mT]	41.33	20.11	14.72	13.65
N_1	18	13	10	10
N_2	2	1	1	1
L_1 [uH]	307.8	287.3	230	240
C_r [nF]	0.082	0.088	0.110	0.106
d_1 [mm]	0.031	0.031	0.033	0.033
d_2 [mm]	0.125	0.126	0.134	0.134
$P_{V,max}$ [kW/m^3]	834	2525	4056	4990
Core name	EQ13	EQ20/R	EQ25	EQ30
P_{core} [W]	2	2	2	2
P_{cu} [W]	0.5	0.5	0.5	0.5
P_V [kW/m^3]	5747	1020	483	402
B_{max} [mT]	37.66	18.33	13.41	12.44
N_1	20	14	11	11
N_2	2	1	1	1
L_1 [uH]	380	333.2	278.3	290.4
C_r [nF]	0.067	0.076	0.091	0.087
d_1 [mm]	0.044	0.045	0.047	0.047
d_2 [mm]	0.181	0.182	0.193	0.193
$P_{V,max}$ [kW/m^3]	834	2525	4056	4990
Core name	EQ13	EQ20/R	EQ25	EQ30
P_{core} [W]	1.25	1.25	1.25	1.25
P_{cu} [W]	1.25	1.25	1.25	1.25
P_V [kW/m^3]	3592	638	302	252
B_{max} [mT]	30.96	15.07	11.03	10.23
N_1	24	17	14	13
N_2	2	2	1	1
L_1 [uH]	547.2	491.3	450.8	405.6
C_r [nF]	0.046	0.0516	0.056	0.062
d_1 [mm]	0.029	0.036	0.032	0.031
d_2 [mm]	0.119	0.147	0.129	0.126
$P_{V,max}$ [kW/m^3]	834	2525	4056	4990

Table B.5: Ferroxcube: EFD core selection.

Core name	EFD 15/8/5	EFD 20/10/7	EFD 25/13/9	EFD 30/15/9
P_{core} [W]	2.5	2.5	2.5	2.5
P_{cu} [W]	1	1	1	1
P_V [kW/m^3]	4902	1712	758	532
B_{max} [mT]	35.25	22.74	16.19	13.97
N_1	28	21	16	15
N_2	3	2	1	1
L_1 [uH]	49.392	27.783	40.96	36
C_r [nF]	0.513	0.912	0.618	0.704
d_1 [mm]	0.049	0.048	0.042	0.044
d_2 [mm]	0.200	0.197	0.172	0.181
$P_{V,max}$ [kW/m^3]	1299	4274	3850	5154
Core name	EFD 15/8/5	EFD 20/10/7	EFD 25/13/9	EFD 30/15/9
P_{core} [W]	2	2	2	2
P_{cu} [W]	0.5	0.5	0.5	0.5
P_V [kW/m^3]	3922	1370	606	426
B_{max} [mT]	32.12	20.72	14.75	12.73
N_1	31	23	17	17
N_2	3	2	2	2
L_1 [uH]	60.543	33.327	46.24	46.24
C_r [nF]	0.418	0.760	0.548	0.548
d_1 [mm]	0.071	0.069	0.074	0.079
d_2 [mm]	0.288	0.283	0.302	0.322
$P_{V,max}$ [kW/m^3]	1299	4274	3850	5154
Core name	EFD 15/8/5	EFD 20/10/7	EFD 25/13/9	EFD 30/15/9
P_{core} [W]	1.25	1.25	1.25	1.25
P_{cu} [W]	1.25	1.25	1.25	1.25
P_V [kW/m^3]	2451	856	379	266
B_{max} [mT]	26.40	17.04	12.13	10.47
N_1	38	28	21	21
N_2	3	3	2	2
L_1 [uH]	90.972	49.392	70.56	70.56
C_r [nF]	0.278	0.513	0.359	0.359
d_1 [mm]	0.047	0.052	0.049	0.052
d_2 [mm]	0.190	0.211	0.198	0.212
$P_{V,max}$ [kW/m^3]	1299	4274	3850	5154

C

Equivalent network without secondary leakage inductance

In Fig. C.1 two networks are shown. It will be derived in this Appendix what the values of L_1, L_2 and M_V must be so that both networks are equivalent. The first network represents a transformer with secondary leakage inductance and the second network does not include a secondary leakage inductance.

The input impedance of the first network is, when the secondary is an open circuit:

$$Z_{oc} = j\omega L_{lk,p} + j\omega L_M \tag{C.1}$$

The input impedance of the second network is, when the secondary is an open circuit:

$$Z_{oc} = j\omega L_1 + j\omega L_2 \tag{C.2}$$

Equating (C.1) and (C.2) gives:

$$L_1 + L_2 = L_{lk,p} + L_M \tag{C.3}$$

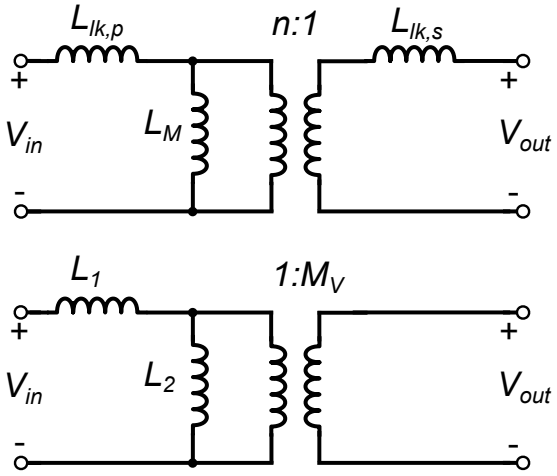


Figure C.1: Equivalence between two transformer networks: one with a secondary leakage inductance and one without.

The input impedance of the first network, when the secondary is a short circuit, is:

$$Z_{sc} = j\omega L_{lk,p} + \frac{j\omega L_M \cdot jn^2\omega L_{lk,s}}{j\omega L_M + jn^2\omega L_{lk,s}} \tag{C.4}$$

The input impedance of the second network, when the secondary is a short circuit, is:

$$Z_{sc} = j\omega L_1 \tag{C.5}$$

Equating (C.4) and (C.5) gives:

$$L_1 = L_{lk,p} + \frac{L_M \cdot jn^2\omega L_{lk,s}}{j\omega L_M + jn^2\omega L_{lk,s}} = L_{lk,p} + \frac{L_M \cdot n^2 L_{lk,s}}{L_M + n^2 L_{lk,s}} \tag{C.6}$$

Thus we found:

$$\boxed{L_1 = L_{lk,p} + L_M//(n^2 L_{lk,s}) = L^e_{sr}} \tag{C.7}$$

From (C.3) we have:

$$\boxed{L_2 = L_{lk,p} + L_M - L_1} \tag{C.8}$$

If we call:

$$\boxed{L^e_{pr} = L_{lk,p} + L_M} \tag{C.9}$$

then the two resonance frequencies of the circuits, if they are at the input connected to a capacitor C_r, are:

$$\boxed{\begin{array}{ll} f^e_{r,1} & = \frac{1}{2\pi\sqrt{L_1 C_r}} = \frac{1}{2\pi\sqrt{L^e_{sr} C_r}} \\ f^e_{r,2} & = \frac{1}{2\pi\sqrt{(L_1+L_2)C_r}} = \frac{1}{2\pi\sqrt{L^e_{pr} C_r}} \end{array}} \tag{C.10}$$

What is now the transformer ratio M_V? The output voltage of the first circuit, when the secondary is an open circuit, is:

$$V_{out,oc} = \frac{1}{n}\frac{j\omega L_M}{j\omega L_M + j\omega L_{lk,p}} V_{in} \tag{C.11}$$

The output voltage of the second circuit, when the secondary is an open circuit, is:

$$V_{out,oc} = M_V \frac{j\omega L_2}{j\omega L_1 + j\omega L_2} V_{in} \tag{C.12}$$

Equating (C.11) and (C.12), and using (C.3) gives:

$$\frac{1}{n}\frac{L_M}{L_M + L_{lk,p}} = M_V \frac{L_2}{L_1 + L_2} = M_V \frac{L_2}{L_{lk,p} + L_M} \tag{C.13}$$

This implies that:

$$M_V L_2 = \frac{L_M}{n} \tag{C.14}$$

Using (C.7) and (C.8) gives:

$$M_V L_2 = \frac{L_M}{n} \Rightarrow M_V = \frac{L_M}{n\left(L_{lk,p} + L_M - L_{lk,p} - L_M//(n^2 L_{lk,s})\right)} \tag{C.15}$$

Simplifying this equation gives:

$$M_V = \frac{L_M}{n\left(L_M - \frac{L_M n^2 L_{lk,s}}{L_M + n^2 L_{lk,s}}\right)} = \frac{1}{n\left(1 - \frac{n^2 L_{lk,s}}{L_M + n^2 L_{lk,s}}\right)} = \frac{L_M + n^2 L_{lk,s}}{n L_M} \tag{C.16}$$

If $n^2 L_{lk,s} = L_{lk,p}$ then we have, with (C.3):

$$M_V = \frac{L_1 + L_2}{n L_M} \tag{C.17}$$

From (C.14) we have that $n^2 M_V L_2 = L_M n$. Using this in (C.17) gives:

$$M_V = \frac{L_1 + L_2}{n^2 M_V L_2} \tag{C.18}$$

Or,

$$\boxed{M_V = \frac{1}{n}\sqrt{\frac{L_1 + L_2}{L_2}}} \tag{C.19}$$

D

Search for the Most Optimal Resonant Tank of the LLC-Converter

Table D.1: Results of the iteration analysis for a transformation ratio of $n = 13$.

n [/]	C_r [nF]	$L_{lk,p}$ [uH]	L_M [uH]	m [/]	$f^e_{r,1}$ [MHz]	f_{min} [MHz]	f_{max} [MHz]	M_{max} [/]	M_{min} [/]	I_{max} [A]	Δf [MHz]	L_{pr} [uH]	L_{sr} [uH]
13	0.25	6	43	4.350	2.999	2.268	2.990	1.396	1.142	0.783	0.722	49	11.265
13	0.25	6	44	4.433	2.997	2.244	2.974	1.396	1.142	0.777	0.730	50	11.280
13	0.3	5	36	4.366	2.999	2.298	2.986	1.396	1.142	0.847	0.688	41	9.390
13	0.37	4	36	5.263	3.001	2.136	2.844	1.396	1.142	0.871	0.708	40	7.600
13	0.37	4	37	5.388	2.999	2.110	2.822	1.396	1.142	0.863	0.712	41	7.610
13	0.37	4	38	5.513	2.998	2.086	2.802	1.396	1.142	0.854	0.716	42	7.619
13	0.49	3	31	5.928	3.002	2.052	2.748	1.396	1.142	0.975	0.696	34	5.735
13	0.49	3	32	6.095	3.000	2.026	2.724	1.396	1.142	0.961	0.698	35	5.743
13	0.5	3	22	4.433	2.997	2.324	2.974	1.396	1.142	1.148	0.650	25	5.640
13	0.74	2	18	5.263	3.001	2.182	2.844	1.396	1.142	1.409	0.662	20	3.800
13	0.74	2	19	5.513	2.998	2.138	2.802	1.396	1.142	1.368	0.664	21	3.810

Table D.2: Results of the iteration analysis for a transformation ratio of $n = 14$.

n [/]	C_r [nF]	$L_{lk,p}$ [uH]	L_M [uH]	m [/]	$f^e_{r,1}$ [MHz]	f_{min} [MHz]	f_{max} [MHz]	M_{max} [/]	M_{min} [/]	I_{max} [A]	Δf [MHz]	L_{pr} [uH]	L_{sr} [uH]
14	0.14	11	52	3.138	3.002	2.366	2.956	1.503	1.230	0.729	0.590	63	20.079
14	0.14	11	53	3.183	3.000	2.334	2.944	1.503	1.230	0.726	0.610	64	20.109
14	0.14	11	54	3.228	2.997	2.302	2.930	1.503	1.230	0.723	0.628	65	20.138
14	0.17	9	46	3.328	3.003	2.364	2.912	1.503	1.230	0.760	0.548	55	16.527
14	0.17	9	47	3.383	3.000	2.340	2.896	1.503	1.230	0.754	0.556	56	16.554
14	0.17	9	48	3.438	2.998	2.314	2.880	1.503	1.230	0.750	0.566	57	16.579
14	0.19	8	45	3.583	3.002	2.300	2.852	1.503	1.230	0.771	0.552	53	14.792
14	0.19	8	46	3.645	3.000	2.276	2.836	1.503	1.230	0.765	0.560	54	14.815
14	0.19	8	47	3.707	2.998	2.250	2.820	1.503	1.230	0.761	0.570	55	14.836
14	0.22	7	33	3.131	3.002	2.486	2.958	1.503	1.230	0.881	0.472	40	12.775
14	0.22	7	34	3.202	2.999	2.458	2.938	1.503	1.230	0.870	0.480	41	12.805
14	0.25	6	42	4.267	3.001	2.160	2.706	1.503	1.230	0.811	0.546	48	11.250
14	0.25	6	43	4.350	2.999	2.136	2.686	1.503	1.230	0.805	0.550	49	11.265
14	0.25	6	44	4.433	2.997	2.114	2.670	1.503	1.230	0.798	0.556	50	11.280
14	0.3	5	35	4.267	3.001	2.192	2.706	1.503	1.230	0.895	0.514	40	9.375
14	0.3	5	36	4.366	2.999	2.166	2.684	1.503	1.230	0.885	0.518	41	9.390
14	0.37	4	36	5.263	3.001	2.008	2.526	1.503	1.230	0.922	0.518	40	7.600
14	0.38	4	23	3.645	3.000	2.368	2.836	1.503	1.230	1.145	0.468	27	7.407
14	0.5	3	21	4.267	3.001	2.230	2.706	1.503	1.230	1.284	0.476	24	5.625
14	0.5	3	22	4.433	2.997	2.192	2.670	1.503	1.230	1.252	0.478	25	5.640
14	0.51	3	16	3.438	2.998	2.430	2.880	1.503	1.230	1.510	0.450	19	5.526
14	0.74	2	18	5.263	3.001	2.054	2.528	1.503	1.230	1.564	0.474	20	3.800
14	0.74	2	19	5.513	2.998	2.010	2.484	1.503	1.230	1.520	0.474	21	3.810
14	0.75	2	14	4.267	3.001	2.240	2.706	1.503	1.230	1.820	0.466	16	3.750

Table D.3: Results of the iteration analysis for a transformation ratio of $n = 15$.

n [/]	C_r [nF]	$L_{lk,p}$ [uH]	L_M [uH]	m [/]	$f^e_{r,1}$ [MHz]	f_{min} [MHz]	f_{max} [MHz]	M_{max} [/]	M_{min} [/]	I_{max} [A]	Δf [MHz]	L_{pr} [uH]	L_{sr} [uH]
15	0.14	11	52	3.138	3.002	2.264	2.772	1.610	1.317	0.733	0.508	63	20.079
15	0.14	11	53	3.183	3.000	2.236	2.758	1.610	1.317	0.730	0.522	64	20.109
15	0.14	11	54	3.228	2.997	2.208	2.744	1.610	1.317	0.726	0.536	65	20.138
15	0.17	9	46	3.328	3.003	2.266	2.724	1.610	1.317	0.773	0.458	55	16.527
15	0.17	9	47	3.383	3.000	2.242	2.706	1.610	1.317	0.767	0.464	56	16.554
15	0.17	9	48	3.438	2.998	2.218	2.690	1.610	1.317	0.762	0.472	57	16.579
15	0.19	8	45	3.583	3.002	2.204	2.660	1.610	1.317	0.789	0.456	53	14.792
15	0.19	8	46	3.645	3.000	2.182	2.642	1.610	1.317	0.782	0.460	54	14.815
15	0.19	8	47	3.707	2.998	2.158	2.626	1.610	1.317	0.777	0.468	55	14.836
15	0.22	7	33	3.131	3.002	2.386	2.776	1.610	1.317	0.917	0.390	40	12.775
15	0.22	7	34	3.202	2.999	2.358	2.754	1.610	1.317	0.905	0.396	41	12.805
15	0.25	6	42	4.267	3.001	2.070	2.506	1.610	1.317	0.842	0.436	48	11.250
15	0.25	6	43	4.350	2.999	2.046	2.488	1.610	1.317	0.836	0.442	49	11.265
15	0.25	6	44	4.433	2.997	2.024	2.468	1.610	1.317	0.828	0.444	50	11.280
15	0.3	5	35	4.267	3.001	2.098	2.506	1.610	1.317	0.944	0.408	40	9.375
15	0.3	5	36	4.366	2.999	2.074	2.484	1.610	1.317	0.931	0.410	41	9.390
15	0.38	4	23	3.645	3.000	2.270	2.644	1.610	1.317	1.233	0.374	27	7.407
15	0.5	3	21	4.267	3.001	2.134	2.508	1.610	1.317	1.397	0.374	24	5.625
15	0.5	3	22	4.433	2.997	2.096	2.470	1.610	1.317	1.362	0.374	25	5.640
15	0.51	3	16	3.438	2.998	2.332	2.692	1.610	1.317	1.650	0.360	19	5.526
15	0.75	2	14	4.267	3.001	2.144	2.508	1.610	1.317	2.007	0.364	16	3.750

Table D.4: Results of the iteration analysis for a transformation ratio of $n = 16$.

n [/]	C_r [nF]	$L_{lk,p}$ [uH]	L_M [uH]	m [/]	$f^e_{r,1}$ [MHz]	f_{min} [MHz]	f_{max} [MHz]	M_{max} [/]	M_{min} [/]	I_{max} [A]	Δf [MHz]	L_{pr} [uH]	L_{sr} [uH]
16	0.14	11	52	3.138	3.002	2.200	2.636	1.718	1.405	0.744	0.436	63	20.079
16	0.14	11	53	3.183	3.000	2.176	2.622	1.718	1.405	0.739	0.446	64	20.109
16	0.14	11	54	3.228	2.997	2.152	2.608	1.718	1.405	0.735	0.456	65	20.138
16	0.17	9	46	3.328	3.003	2.196	2.586	1.718	1.405	0.794	0.390	55	16.527
16	0.17	9	47	3.383	3.000	2.174	2.568	1.718	1.405	0.787	0.394	56	16.554
16	0.17	9	48	3.438	2.998	2.152	2.552	1.718	1.405	0.780	0.400	57	16.579
16	0.19	8	45	3.583	3.002	2.138	2.520	1.718	1.405	0.812	0.382	53	14.792
16	0.19	8	46	3.645	3.000	2.116	2.502	1.718	1.405	0.805	0.386	54	14.815
16	0.19	8	47	3.707	2.998	2.094	2.484	1.718	1.405	0.799	0.390	55	14.836
16	0.22	7	33	3.131	3.002	2.310	2.640	1.718	1.405	0.961	0.330	40	12.775
16	0.22	7	34	3.202	2.999	2.284	2.618	1.718	1.405	0.946	0.334	41	12.805
16	0.25	6	42	4.267	3.001	2.002	2.364	1.718	1.405	0.881	0.362	48	11.250
16	0.3	5	35	4.267	3.001	2.028	2.364	1.718	1.405	0.997	0.336	40	9.375
16	0.3	5	36	4.366	2.999	2.004	2.342	1.718	1.405	0.984	0.338	41	9.390
16	0.38	4	23	3.645	3.000	2.194	2.504	1.718	1.405	1.326	0.310	27	7.407
16	0.5	3	21	4.267	3.001	2.060	2.366	1.718	1.405	1.514	0.306	24	5.625
16	0.5	3	22	4.433	2.997	2.022	2.328	1.718	1.405	1.476	0.306	25	5.640
16	0.51	3	16	3.438	2.998	2.256	2.554	1.718	1.405	1.793	0.298	19	5.526
16	0.75	2	14	4.267	3.001	2.068	2.366	1.718	1.405	2.200	0.298	16	3.750

Table D.5: Results of the iteration analysis for a transformation ratio of $n = 17$.

n [/]	C_r [nF]	$L_{lk,p}$ [uH]	L_M [uH]	m [/]	$f^e_{r,1}$ [MHz]	f_{min} [MHz]	f_{max} [MHz]	M_{max} [/]	M_{min} [/]	I_{max} [A]	Δf [MHz]	L_{pr} [uH]	L_{sr} [uH]
17	0.14	11	52	3.138	3.002	2.156	2.532	1.825	1.493	0.758	0.376	63	20.079
17	0.14	11	53	3.183	3.000	2.134	2.516	1.825	1.493	0.753	0.382	64	20.109
17	0.14	11	54	3.228	2.997	2.112	2.502	1.825	1.493	0.749	0.390	65	20.138
17	0.17	9	46	3.328	3.003	2.146	2.480	1.825	1.493	0.818	0.334	55	16.527
17	0.17	9	47	3.383	3.000	2.124	2.462	1.825	1.493	0.811	0.338	56	16.554
17	0.17	9	48	3.438	2.998	2.104	2.446	1.825	1.493	0.803	0.342	57	16.579
17	0.19	8	45	3.583	3.002	2.086	2.412	1.825	1.493	0.843	0.326	53	14.792
17	0.19	8	46	3.645	3.000	2.064	2.396	1.825	1.493	0.836	0.332	54	14.815
17	0.19	8	47	3.707	2.998	2.044	2.378	1.825	1.493	0.828	0.334	55	14.836
17	0.22	7	33	3.131	3.002	2.252	2.536	1.825	1.493	1.009	0.284	40	12.775
17	0.22	7	34	3.202	2.999	2.226	2.512	1.825	1.493	0.993	0.286	41	12.805
17	0.38	4	23	3.645	3.000	2.134	2.398	1.825	1.493	1.423	0.264	27	7.407
17	0.51	3	16	3.438	2.998	2.196	2.450	1.825	1.493	1.936	0.254	19	5.526
17	0.75	2	14	4.267	3.001	2.008	2.258	1.825	1.493	2.393	0.250	16	3.750

Table D.6: Results of the iteration analysis for a transformation ratio of $n = 18$.

n [/]	C_r [nF]	$L_{lk,p}$ [uH]	L_M [uH]	m [/]	$f^e_{r,1}$ [MHz]	f_{min} [MHz]	f_{max} [MHz]	M_{max} [/]	M_{min} [/]	I_{max} [A]	Δf [MHz]	L_{pr} [uH]	L_{sr} [uH]
18	0.14	11	52	3.138	3.002	2.122	2.448	1.932	1.581	0.778	0.326	63	20.079
18	0.14	11	53	3.183	3.000	2.102	2.434	1.932	1.581	0.772	0.332	64	20.109
18	0.14	11	54	3.228	2.997	2.082	2.418	1.932	1.581	0.766	0.336	65	20.138
18	0.17	9	46	3.328	3.003	2.106	2.396	1.932	1.581	0.847	0.290	55	16.527
18	0.17	9	47	3.383	3.000	2.084	2.380	1.932	1.581	0.841	0.296	56	16.554
18	0.17	9	48	3.438	2.998	2.064	2.362	1.932	1.581	0.833	0.298	57	16.579
18	0.19	8	45	3.583	3.002	2.046	2.328	1.932	1.581	0.876	0.282	53	14.792
18	0.19	8	46	3.645	3.000	2.026	2.312	1.932	1.581	0.867	0.286	54	14.815
18	0.19	8	47	3.707	2.998	2.006	2.294	1.932	1.581	0.859	0.288	55	14.836
18	0.22	7	33	3.131	3.002	2.204	2.452	1.932	1.581	1.062	0.248	40	12.775
18	0.22	7	34	3.202	2.999	2.180	2.430	1.932	1.581	1.044	0.250	41	12.805
18	0.38	4	23	3.645	3.000	2.086	2.314	1.932	1.581	1.521	0.228	27	7.407
18	0.51	3	16	3.438	2.998	2.146	2.366	1.932	1.581	2.082	0.220	19	5.526

Table D.7: Results of the iteration analysis for a transformation ratio of $n = 19$.

n [/]	C_r [nF]	$L_{lk,p}$ [uH]	L_M [uH]	m [/]	$f^e_{r,1}$ [MHz]	f_{min} [MHz]	f_{max} [MHz]	M_{max} [/]	M_{min} [/]	I_{max} [A]	Δf [MHz]	L_{pr} [uH]	L_{sr} [uH]
19	0.14	11	52	3.138	3.002	2.094	2.380	2.040	1.669	0.802	0.286	63	20.079
19	0.14	11	53	3.183	3.000	2.076	2.366	2.040	1.669	0.794	0.290	64	20.109
19	0.14	11	54	3.228	2.997	2.056	2.352	2.040	1.669	0.789	0.296	65	20.138
19	0.17	9	46	3.328	3.003	2.072	2.328	2.040	1.669	0.882	0.256	55	16.527
19	0.17	9	47	3.383	3.000	2.052	2.312	2.040	1.669	0.873	0.260	56	16.554
19	0.17	9	48	3.438	2.998	2.034	2.294	2.040	1.669	0.863	0.260	57	16.579
19	0.19	8	45	3.583	3.002	2.012	2.260	2.040	1.669	0.915	0.248	53	14.792
19	0.22	7	33	3.131	3.002	2.166	2.386	2.040	1.669	1.117	0.220	40	12.775
19	0.22	7	34	3.202	2.999	2.140	2.362	2.040	1.669	1.100	0.222	41	12.805
19	0.38	4	23	3.645	3.000	2.046	2.246	2.040	1.669	1.620	0.200	27	7.407
19	0.51	3	16	3.438	2.998	2.104	2.298	2.040	1.669	2.231	0.194	19	5.526

Table D.8: Results of the iteration analysis for a transformation ratio of $n = 20$.

n [/]	C_r [nF]	$L_{lk,p}$ [uH]	L_M [uH]	m [/]	$f^e_{r,1}$ [MHz]	f_{min} [MHz]	f_{max} [MHz]	M_{max} [/]	M_{min} [/]	I_{max} [A]	Δf [MHz]	L_{pr} [uH]	L_{sr} [uH]
20	0.14	11	52	3.138	3.002	2.072	2.324	2.147	1.757	0.826	0.252	63	20.079
20	0.14	11	53	3.183	3.000	2.052	2.310	2.147	1.757	0.821	0.258	64	20.109
20	0.14	11	54	3.228	2.997	2.034	2.294	2.147	1.757	0.815	0.260	65	20.138
20	0.17	9	46	3.328	3.003	2.044	2.272	2.147	1.757	0.918	0.228	55	16.527
20	0.17	9	47	3.383	3.000	2.026	2.256	2.147	1.757	0.907	0.230	56	16.554
20	0.17	9	48	3.438	2.998	2.006	2.238	2.147	1.757	0.900	0.232	57	16.579
20	0.22	7	33	3.131	3.002	2.132	2.330	2.147	1.757	1.177	0.198	40	12.775
20	0.22	7	34	3.202	2.999	2.108	2.306	2.147	1.757	1.156	0.198	41	12.805
20	0.38	4	23	3.645	3.000	2.010	2.190	2.147	1.757	1.727	0.180	27	7.407
20	0.51	3	16	3.438	2.998	2.068	2.242	2.147	1.757	2.382	0.174	19	5.526

E

Test Results to Determine the Equivalent Model of the Transformer of the LLC-Converter

E.1 Results of the open-circuit test

Table E.1: Input impedance of the transformer of the LLC-converter, measured with the secondary side an open-circuit.

frequency [Hz]	Re(Z) [Ω]	Im(Z) [Ω]	L_1 [μH]	phase(Z) [°]
300000	0.21291	52.674	27.944	89.77
400000	0.1953	70.348	27.991	89.84
500000	0.2578	88.074	28.035	89.83
600000	0.4141	106.01	28.120	89.78
700000	0.3711	124.08	28.211	89.83
800000	0.477	142.49	28.347	89.81
900000	0.43	161.01	28.473	89.87
1000000	0.961	179.82	28.619	89.69
1100000	0.93	198.83	28.768	89.73
1200000	1.078	218.51	28.981	89.72
1300000	1.195	238.28	29.172	89.71
1400000	1.5	258.44	29.380	89.67
1500000	1.688	279.42	29.647	89.65
1600000	2.938	300.73	29.914	89.44
1700000	2.313	322.91	30.231	89.59
1800000	2.031	344.84	30.491	89.66
1900000	2.953	367	30.742	89.539
2000000	2.703	392	31.194	89.60
2100000	3.813	417.72	31.658	89.48
2200000	4.391	442.23	31.992	89.43
2300000	4.344	469.23	32.470	89.47
2400000	6.25	496.66	32.936	89.28
2500000	6.531	526.69	33.530	89.29
2600000	7.375	556.91	34.091	89.24
2700000	8.5	587.56	34.634	89.17
2800000	10.063	619.69	35.224	89.07
2900000	12.563	654.62	35.926	88.90
3000000	16.25	692.88	36.758	88.66
3300000	22.938	813.88	39.252	88.39
3600000	41.75	961.78	42.520	87.51
3900000	54	1140.1	46.526	87.29
4200000	71.69	1372.9	52.025	87.01
4500000	122.25	1671.1	59.103	85.82
4800000	188.63	2106.1	69.833	84.88
5100000	321.25	2750.3	85.828	83.34
5200000	401.75	3047.5	93.274	82.49
5300000	519.87	3412.9	102.487	81.34
5400000	631.25	3797.1	111.913	80.56
5500000	893.25	4440.8	128.505	78.63
5600000	1245	5232.8	148.719	76.62
5700000	1550.8	6250	174.512	76.06
5800000	2704.8	7422	203.663	69.98
5900000	4497	8794	237.222	62.92
6000000	8361	9967	264.383	50.01
6050000	10873	10922	287.321	45.13

Table E.1: Input impedance of the transformer of the LLC-converter, measured with the secondary side an open-circuit.

frequency [Hz]	Re(Z) [Ω]	Im(Z) [Ω]	L_1 [μH]	phase(Z) [°]
6075000	12518	11671	305.761	42.99
6100000	14384	12245	319.484	40.41
6125000	16658	11644	302.563	34.95
6150000	18355	8946	231.512	25.98
6200000	19364	3314	85.071	9.71
6250000	18228	-2493	-63.484	-7.79
6300000	14700	-6503	-164.283	-23.86
6350000	12169	-8988.5	-225.286	-36.45
6400000	9441	-10332	-256.936	-47.58
6450000	6840	-9768.5	-241.040	-55.0
6500000	4991	-8822	-216.010	-60.50
6600000	3509	-7320.7	-176.534	-64.39
6700000	2682.5	-6337.3	-150.539	-67.06
6800000	1948	-5586.8	-130.760	-70.78
6900000	1628	-4783	-110.324	-71.20
7200000	753.87	-3576.8	-79.065	-78.10
7500000	494.75	-2782.9	-59.055	-79.92
7800000	341.88	-2373.3	-48.426	-81.80
8100000	195.81	-2033.7	-39.960	-84.50
8400000	173.63	-1740.4	-32.975	-84.30
8700000	132.69	-1575.7	-28.825	-85.19
9000000	113.94	-1433.7	-25.353	-85.46
9500000	83.81	-1240.1	-20.776	-86.14
10000000	71.13	-1100.4	-17.513	-86.30
10500000	62.844	-979.94	-14.854	-86.33
11000000	54.969	-898.94	-13.006	-86.50
11500000	48.688	-820.16	-11.351	-86.60
12000000	39.125	-765.37	-10.151	-87.07
12500000	34.938	-707.75	-9.011	-87.17
13000000	32.719	-669.28	-8.194	-87.20
13500000	28.25	-627.25	-7.395	-87.42
14000000	27.438	-591.97	-6.730	-87.35
14500000	25.688	-561	-6.158	-87.38
15000000	21.031	-534.12	-5.667	-87.75
15500000	20.922	-509.08	-5.227	-87.65
16000000	19.75	-485.08	-4.825	-87.67
16500000	18.656	-464.16	-4.477	-87.70
17000000	17.547	-443.14	-4.149	-87.73
17500000	16.703	-426.34	-3.877	-87.76
18000000	18.234	-409.45	-3.620	-87.45

E.2 Results of the short-circuit test

Table E.2: Input impedance of the transformer of the LLC-converter, measured with the two secondary coils in series and short-circuited.

frequency [Hz]	Re(Z) [Ω]	Im(Z) [Ω]	L_1 [μH]	phase(Z) [°]
300000	1.459	13.696	7.266	83.92
400000	1.9121	18.045	7.180	83.95
500000	1.6973	22.662	7.214	85.72
600000	2.0938	26.983	7.157	85.56
700000	1.9258	31.632	7.192	86.51
800000	2.3008	35.941	7.150	86.34
900000	2.2148	40.609	7.181	86.88
1000000	2.549	44.939	7.152	86.75
1100000	2.4868	49.641	7.182	87.13
1200000	2.7832	53.998	7.162	87.05
1300000	2.7656	58.717	7.189	87.30
1400000	3.0703	63.117	7.175	87.22
1500000	3.1328	67.863	7.200	87.36
1600000	3.3984	72.254	7.187	87.31
1700000	3.4531	76.988	7.208	87.43
1800000	3.6914	81.566	7.212	87.41
1900000	3.7461	86.461	7.242	87.52
2000000	4.0547	91.066	7.247	87.45
2100000	4.2227	95.973	7.274	87.48
2200000	4.4922	100.6	7.278	87.44
2300000	4.625	105.54	7.303	87.49
2400000	4.8594	110.4	7.321	87.48
2500000	5.0156	115.52	7.354	87.51
2600000	5.3242	120.35	7.367	87.47
2700000	5.5664	125.46	7.395	87.46
2800000	5.859	130.49	7.417	87.43
2900000	6.078	135.76	7.451	87.44
3000000	6.445	140.89	7.474	87.38
3500000	8.188	158.29	7.198	87.04
4000000	10.227	197.7	7.866	87.04
4500000	12.695	229.69	8.124	86.84
5000000	15.391	263.44	8.386	86.66
5500000	18.609	302.66	8.758	86.48
6000000	24.219	347.91	9.2299	86.02
6500000	29.688	399.17	9.774	85.75
7000000	38.531	458.16	10.417	85.197
7500000	50.156	529.53	11.237	84.59
8000000	67.125	618.75	12.310	83.81
8500000	91.688	728.13	13.634	82.82
9000000	123.94	866.22	15.318	81.86
9500000	190.5	1057.5	17.716	79.79
10000000	296.88	1322.6	21.050	77.35
10500000	537.13	1730.5	26.230	72.76
11000000	1133.6	2294	33.191	63.70
11100000	1326.8	2470.4	35.421	61.76

Table E.2: Input impedance of the transformer of the LLC-converter, measured with the two secondary coils in series and short-circuited.

frequency [Hz]	Re(Z) [Ω]	Im(Z) [Ω]	L_1 [μH]	phase(Z) [°]
11200000	1574.6	2693.5	38.275	59.69
11300000	1941.4	2833.6	39.910	55.58
11400000	2396.1	2903.5	40.536	50.47
11500000	2828.1	3072.6	42.523	47.37
11600000	3346.6	3274.4	44.926	44.38
11700000	4192.5	2903.3	39.494	34.70
11800000	4944.3	2068.8	27.903	22.71
11900000	5516.3	1164.3	15.572	11.92
12000000	5778.5	103.5	1.373	1.03
12050000	5834	-425	-5.613	-4.17
12100000	5792.5	-963	-12.667	-9.44
12150000	5683.2	-1476	-19.334	-14.56
12200000	5471	-1944.8	-25.371	-19.57
12300000	4669.3	-2543.8	-32.915	-28.58
12400000	3882.4	-2807	-36.028	-35.87
12500000	3178.6	-2992.1	-38.100	-43.27
12600000	2575.9	-3016.3	-38.100	-49.50
12700000	2186	-2910	-36.468	-53.09
12800000	1886.5	-2775.6	-34.512	-55.80
12900000	1605.8	-2590.6	-31.962	-58.21
13000000	1382.4	-2413.3	-29.545	-60.19
13300000	910.75	-2135.8	-25.558	-66.91
13600000	640.94	-1822.4	-21.327	-70.62
13900000	482.94	-1605.9	-18.388	-73.26
14200000	349.06	-1399	-15.680	-75.99
14500000	275.75	-1277.7	-14.024	-77.82
15000000	227.63	-1097.4	-11.644	-78.28
16000000	122.91	-839.06	-8.346	-81.67
17000000	90.406	-690	-6.460	-82.54
18000000	67	-587.56	-5.195	-83.49
19000000	56.25	-512.69	-4.295	-83.74
20000000	46.734	-452.56	-3.601	-84.10
21000000	41.047	-406.94	-3.084	-84.24
22000000	35.313	-367.31	-2.657	-84.51
23000000	30.547	-334.95	-2.318	-84.79
24000000	28.688	-308.23	-2.044	-84.68
25000000	27.531	-287.91	-1.833	-84.54
26000000	26.313	-263.47	-1.613	-84.30
27000000	25.492	-244.58	-1.442	-84.05
28000000	25.07	-228.16	-1.297	-83.73
29000000	24.984	-212.57	-1.167	-83.30
30000000	25.234	-198.12	-1.051	-82.74
31000000	25.875	-184.59	-0.948	-82.02
32000000	27.016	-172.09	-0.856	-81.08
33000000	28.359	-160.2	-0.773	-79.96
34000000	30.063	-149.32	-0.700	-78.62
35000000	31.586	-138.52	-0.630	-77.15
36000000	33.809	-127.56	-0.564	-75.16
37000000	36.883	-116.79	-0.502	-72.47

Table E.2: Input impedance of the transformer of the LLC-converter, measured with the two secondary coils in series and short-circuited.

frequency [Hz]	Re(Z) [Ω]	Im(Z) [Ω]	L_1 [μH]	phase(Z) [°]
38000000	40.883	-106.28	-0.445	-68.96
39000000	45.93	-95.668	-0.390	-64.35
40000000	52	-85.344	-0.334	-58.65

E.3 Measuring the frequency-dependence of the Litz-wire, used for the windings of the transformer

Table E.3: Frequency-dependent resistance of a Litz-wire consisting of 54 strands AWG44.

frequency [Hz]	Re(Z_{in}) [Ω]	R(connector) [Ω]	R(wire) [Ω]
300000	0.11426	0.030512	0.083748
500000	0.11633	0.033527	0.082803
700000	0.12793	0.039532	0.088398
900000	0.1377	0.04397	0.09373
1100000	0.15186	0.05453	0.09733
1300000	0.13379	0.03313	0.10066
1500000	0.16138	0.04961	0.11177
1700000	0.13379	0.02505	0.10874
1900000	0.1626	0.04647	0.11613
2100000	0.16943	0.05064	0.11879
2300000	0.18018	0.04907	0.13111
2500000	0.17773	0.0397	0.13803
2700000	0.20166	0.05298	0.14868
2900000	0.18213	0.04205	0.14008
3000000	0.20605	0.05399	0.15206
4000000	0.25195	0.05875	0.1932
5000000	0.2881	0.05029	0.23781
6000000	0.3252	0.05084	0.27436
7000000	0.4063	0.09155	0.31475
8000000	0.3936	0.05466	0.33894
9000000	0.4521	0.08096	0.37114
10000000	0.4707	0.05542	0.41528
11000000	0.5137	0.06982	0.44388
12000000	0.4941	0.05463	0.43947
13000000	0.5332	0.05219	0.48101
14000000	0.582	0.0889	0.4931
15000000	0.6934	0.08051	0.61289
16000000	0.6895	0.09497	0.59453
17000000	0.709	0.09387	0.61513

18000000	0.709	0.0885	0.6205
19000000	0.7578	0.09387	0.66393
20000000	0.7383	0.099	0.6393
21000000	0.8789	0.10376	0.77514
22000000	0.8711	0.10181	0.76929
23000000	1.0195	0.10474	0.91476
24000000	0.9961	0.11316	0.88294
25000000	1.1602	0.09021	1.06999

F

MOSFET Selection

Table F.1: Overview of candidate MOSFETs, ordered according to increasing gate charge.

MOSFET	$BVDSS$ **[V]**	$I_{ds,max}$ **[A], at** $T_c = 25°$**C**	Q_g **[nC]**	$R_{on,stat}$ [Ω]	$Coss$ **[pF] at** $V_{gs} = 0$ **V,** $V_{ds} = 25$ **V,** $f = 1$ **MHz**	$R_{on,stat} \cdot Q_g$ [Ω.**nC**]
STD3NM50	500	3	5.5	2.5	40	13.75
FDD4N50	600	3.4	8.3	1.9	40	15.77
FQP2N60C	600	2	8.5	3.6	20	30.6
FQP4N50	500	3.4	10	2	55	20
FDD5N50	500	4	11	1.15	66	12.65
STF4N52K3	525	2.5	11	2.1	20 eff.	23.1
STP4NK50Z	500	3	12	2.3	33	27.6
STD4NK50ZD-1	500	3	12	2.3	49	27.6
SPP03N60S5	600	3.2	12.4	1.25	150	15.5
FDD6N50	500	6	12.8	0.76	95	9.728
IRFU420	500	2.5	13	2.9	54	37.7
IXTY3N50P	500	3.6	14.88	2	48	29.76
STF5N52K3	525	4.4	17	1.2	33 eff.	20.4
IRF820APbF	500	2.5	17	3	28 eff.	51
IRFC20	600	2	18	4.4	92	79.2
IRFR420PbF	500	2.4	19	3	92	57
BUZ74	500	2.4	24.8	2.5	50	62
IRFI830G	500	3.1	38	1.5	160	57

G

Altium Layout of the Half-Bridge Gate-Driver for the LLC-Converter

Table G.1: Bill of materials of the half-bridge gate-driver for the LLC-converter.

Footprint	Library reference	Designator	Description	Quantity
smd C0805_0.60	CSMD805/100pF	C1, C2	smd capacitor, 0805, 100pF	2
smd C0805_0.85	CSMD805/100nF	C3, C4, C6, C8	smd capacitor, 0805, 100nF	4
smd C1210	CSMD1210P /22uF/25V	C5, C7, C9, C13, C15	smd capacitor, 1210, 22uF/25V	5
con SMA/G	CON SMA/G	CON1	SMA connector, right-angled, 50 Ohm	1
hdr 1x8	CON HDR 1x8	CON2	pcb header straight, 1x8 pitch 100mil	1

Table G.1: Bill of materials of the half-bridge gate-driver for the LLC-converter.

Footprint	**Library reference**	**Designator**	**Description**	**Quantity**
hdr 1x2	CON HDR 1x2	CON3	pcb header, straight, 1x2 pitch 100mil	1
SOD-323	BAS170W	D1, D2	Silicon AF Schottky Diode for High-Speed Switching	2
DIP 8 pins	TC4427	U100, U101	1.5A high-speed mosfet driver	2
smd SOICN/8	ADUM1200CRZ	IC2, IC3	Digital Isolator, 2 channel	2
IL0512s	IL0512S	IC5, IC6	DC/DC CONVERTER, 2W, SINGLE O/P, 5->12V	2
TO-92	LM78L05ACZ	IC7, IC8	low-power voltage regulator, +5V, TO-92	2
smd C1206_0.55	4R7/1206	R3, R4	resistor, SMD1206, 4R7	2
smd C0805_0.50	50R/805	R5	resistor, SMD805, 50R	1
trimmer R/V/1T (BOURNS 3299W)	TMV25T/20K	TM1, TM2	trimmer, vertical, 25 turns, 20K	2
646-06	MC74ACT86N	U1	Quad 2-Input XOR Gate	1

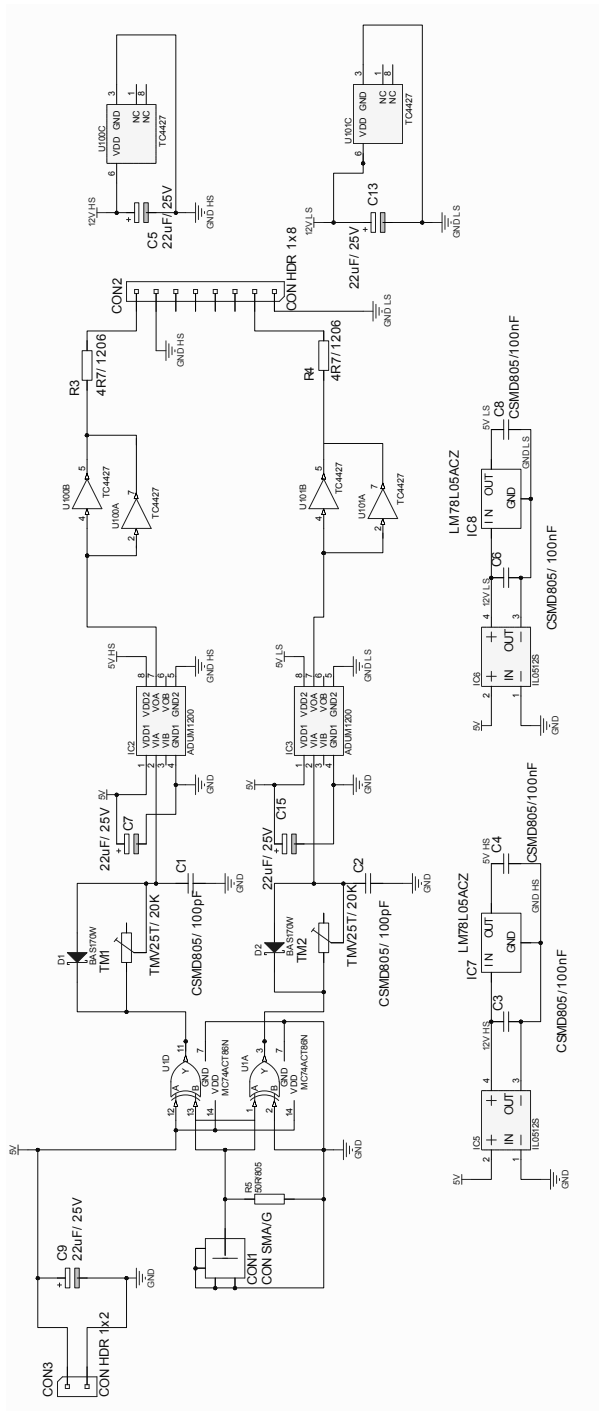


Figure G.1: Altium layout of the half-bridge gate-driver for the LLC-converter.

H

Derivation of the PEEC-equation

The electric field $\vec{E}$ in a point $\vec{r}$ in a metallic conductor is the sum of an externally applied incident field $\vec{E}_i$ and the field scattered by electric sources, which are charges and currents, present on and inside the conductor structure, $\vec{E}_s$ [Harr 68]:

$$\vec{E}(\vec{r},t) = \vec{E}_i + \vec{E}_s \tag{H.1}$$

For conductors,

$$\vec{E} = \frac{\vec{J}}{\sigma} \tag{H.2}$$

where σ is the electric conductivity at the point and $\vec{J}$ is the current density (unit: $\mathrm{A/m^2}$). In general, the scattered field is [Harr 68]:

$$\vec{E}_s = -\vec{\nabla}\phi - \frac{\partial \vec{A}}{\partial t} \tag{H.3}$$

where ϕ is the electric scalar potential and $\vec{A}$ is the magnetic vector potential. These two potentials are functions of the charges and currents respectively. More precisely, for a system of K conductors, composing an electric circuit,

they can be written as follows:

$$\phi(\vec{r},t) = \frac{1}{4\pi\epsilon}\sum_{k=1}^{K}\int_{V_k}\frac{\rho(\vec{r'},t-R/v)}{R}dV' \tag{H.4}$$

$$\vec{A}(\vec{r},t) = \frac{\mu}{4\pi}\sum_{k=1}^{K}\int_{V_k}\frac{\vec{J}(\vec{r'},t-R/v)}{R}dV' \tag{H.5}$$

where ϵ and μ are the permittivity and permeability of the medium where the conductors are located in. The assumption that was made and allows to write previous equations, is that this medium is homogeneous and isotropic. $\vec{r'}$ is a point in the volume V_k of the k^{th} conductor. It can be noticed that the integration is done over the volume of the conductors, containing the electromagnetic sources, the charges and currents. ρ is the volume charge density (units: C/m^3). R is the distance between the source point and the observation point: $R = |\vec{r} - \vec{r'}|$. v is the speed of electromagnetic waves in the medium surrounding the conductors. These potentials, ϕ and $\vec{A}$, are also called 'retarded potentials' because the sources that produce them must be evaluated at a previous time instance, corresponding to the time it takes for the electromagnetic waves to propagate from the source to the observation point.

We thus have for the incident field at a point $\vec{r}$ inside the metallic structure and at time t:

$$\vec{E}_i(\vec{r},t) = \frac{\vec{J}(\vec{r},t)}{\sigma} + \vec{\nabla}\phi(\vec{r},t) + \frac{\partial\vec{A}(\vec{r},t)}{\partial t} \tag{H.6}$$

Inserting equations (H.4) and (H.5) into (H.6) gives:

$$\frac{\vec{J}(\vec{r},t)}{\sigma} + \sum_{k=1}^{K}\frac{1}{4\pi\epsilon}\vec{\nabla}\left[\int_{V_k}\frac{\rho(\vec{r'},t-\frac{R}{v})}{R}dV'\right]$$

$$+\frac{\partial}{\partial t}\sum_{k=1}^{K}\frac{\mu}{4\pi}\int_{V_k}\frac{\vec{J}(\vec{r'},t-\frac{R}{v})}{R}dV' = \vec{E}_i(\vec{r},t) \tag{H.7}$$

Equation (H.7) is called an electric field integral equation (EFIE) [Ekma 03]. From now on, we shall denote $t - R/v$ by t'. We can also write this for each component (x, y, z) separately:

$$\frac{J_\gamma(\vec{r},t)}{\sigma} + \sum_{k=1}^{K}\frac{1}{4\pi\epsilon}\frac{\partial}{\partial\gamma}\left[\int_{V_k}\frac{\rho(\vec{r'},t')}{R}dV'\right]$$

$$+\frac{\partial}{\partial t}\sum_{k=1}^{K}\frac{\mu}{4\pi}\int_{V_k}\frac{J_\gamma(\vec{r'},t')}{R}dV' = E_{i,\gamma}(\vec{r},t) \tag{H.8}$$

where $\gamma = x$ or y or z. In order to solve (H.8), the metallic conductors are subdivided in smaller volume segments (called inductive subdivisions, for reasons that will become clear later on) where the current density is approximately constant. Furthermore, the surface of the metallic conductors is subdivided in smaller surface segments (called capacitive subdivisions) where the charge density is approximately constant. There are Q_k surface cells on conductor k and $N_{\gamma,k}$ volume cells on conductor k, associated with the component γ. We can approximate the γ-component of the current density in and the charge density on conductor k as follows:

$$J_{\gamma,k}(\vec{r'},t') \approx \sum_{n=1}^{N_{\gamma,k}} P^V_{\gamma,n,k} J_{\gamma,n,k}(t_n) \tag{H.9}$$

$$\rho_k(\vec{r'},t') \approx \sum_{q=1}^{Q_k} P^S_{q,k} \rho_{q,k}(t_q) \tag{H.10}$$

where $t_n = t - |\vec{r} - \vec{r'}_n|/v$ and $t_q = t - |\vec{r} - \vec{r'}_q|/v$ and $\vec{r'}_n$ is the position vector of the centre of the n^{th} inductive subdivision of conductor k and $\vec{r'}_q$ is the position vector of the centre of the q^{th} capacitive subdivision of conductor k. P^V and P^S are unit pulse functions, defined on respectively an inductive subdivision (a volume) and a capacitive subdivision (a surface):

$$P^V_{\gamma,n,k} = 1, \quad \text{inside the } n^{\text{th}} \text{ volume cell of the } k^{\text{th}} \text{ conductor} \tag{H.11}$$

$$= 0, \quad \text{elsewhere} \tag{H.12}$$

$$P^S_{q,k} = 1, \quad \text{on the } q^{\text{th}} \text{ surface cell of the } k^{\text{th}} \text{ conductor} \tag{H.13}$$

$$= 0, \quad \text{elsewhere} \tag{H.14}$$

Here, it is assumed that the charges are present on the surface of the conductors only. Substituting (H.9) in (H.8), gives, for component γ:

$$\frac{J_\gamma(\vec{r},t)}{\sigma} + \sum_{k=1}^{K} \frac{1}{4\pi\epsilon} \frac{\partial}{\partial\gamma} \left[\int_{V_k} \frac{\rho(\vec{r'},t')}{R} dV' \right] +$$

$$\frac{\partial}{\partial t} \sum_{k=1}^{K} \sum_{n=1}^{N_{\gamma,k}} \frac{\mu}{4\pi} \left[\int_{V_k} \frac{P^V_{\gamma,n,k} J_{\gamma,n,k}(t_n)}{R} dV' \right] \approx E_{i,\gamma}(\vec{r},t) \tag{H.15}$$

Because of the unit pulse function, the integral over V_k of the unit pulse $P^V_{\gamma,n,k}$ multiplied with a function $(J_{\gamma,n,k}/R)$ is equal to the integral over $V_{\gamma,n,k}$ (=the

n^{th} volume cell associated with direction γ, on conductor k) of the latter function:

$$\frac{J_\gamma(\vec{r},t)}{\sigma} + \sum_{k=1}^{K} \frac{1}{4\pi\epsilon} \frac{\partial}{\partial\gamma} \left[\int_{V_k} \frac{\rho(\vec{r'},t')}{R} dV' \right] +$$

$$\frac{\partial}{\partial t} \sum_{k=1}^{K} \sum_{n=1}^{N_{\gamma,k}} \frac{\mu}{4\pi} \left[\int_{V_{\gamma,n,k}} \frac{J_{\gamma,n,k}(t_n)}{R} dV'_{\gamma,n,k} \right] \approx E_{i,\gamma}(\vec{r},t) \tag{H.16}$$

Furthermore, because the charge density only exists on the surface, the integral over the volume V_k, is actually the integral over the surface S_k if we change the unit of the charge density ρ from C/m^3 to C/m^2 (new symbol: ρ'):

$$\frac{J_\gamma(\vec{r},t)}{\sigma} + \sum_{k=1}^{K} \frac{1}{4\pi\epsilon} \frac{\partial}{\partial\gamma} \left[\int_{S_k} \frac{\rho'(\vec{r'},t')}{R} dS' \right] +$$

$$\frac{\partial}{\partial t} \sum_{k=1}^{K} \sum_{n=1}^{N_{\gamma,k}} \frac{\mu}{4\pi} \left[\int_{V_{\gamma,n,k}} \frac{J_{\gamma,n,k}(t_n)}{R} dV'_{\gamma,n,k} \right] \approx E_{i,\gamma}(\vec{r},t) \tag{H.17}$$

We will next 'weigh' the obtained equation according to the Galerkin procedure.

Intermezzo: Galerkin weighing [Gibs 07]

Suppose we have an integral equation, differential equation or mixed integro-differential equation, in fact any equation where a linear operator L is present:

$$Ly(x) = f(x), \qquad a \le x \le b \tag{H.18}$$

or:

$$Ly(x) - f(x) = 0 \tag{H.19}$$

$f(x)$ is the known 'excitation' function and $y(x)$ represents the unknown 'response'. We wish to determine $y(x)$. We approximate $y(x)$ as a sum of basis functions $b_i(x)$:

$$u(x) = \sum_{i=1}^{N} c_i b_i(x) \tag{H.20}$$

And we require that $u(x) \approx y(x)$[1]. This may be an exact equality, or an approximation. The basis functions may be pulse functions, triangles, sines and cosines, Bessel functions, etc. We then have:

$$Lu(x) - f(x) = \sum_{i=1}^{N} c_i L(b_i(x)) - f(x) = r(x) \tag{H.21}$$

[1] Also an infinite number of terms in the series of $u(x)$ is possible.

$r(x)$ is called 'the residue'. In order for $u(x)$ to (better) represent $y(x)$, the residue should be as close to zero as possible, for all x. One technique is requiring that the residue is exactly zero in the spatial discretization points: $r(x_i) = 0, \forall x_i$. This is called '*point weighing*'. Another way of saying that 'the residue is small', is by using weighing functions $w_j(x)$, weighing the residue with these functions and integrating this weighed residue over the solution domain. The integral of the weighed residue is then put to zero:

$$\int_a^b w_j(x) r(x) dx = 0 \tag{H.22}$$

The weighing procedure is also called 'testing' and the functions $w_j(x)$ are also called *test functions*. Note that the point weighing technique can also be seen as a form of weighing, where the test functions are Dirac impulses. We thus have:

$$\int_a^b w_j(x) \sum_{i=1}^{N} c_i L(b_i(x)) dx = \int_a^b w_j(x) f(x) dx \tag{H.23}$$

So, in order to determine the N unknown coefficient c_i, we require N equations, thus we need N weighing functions. In the Galerkin procedure, named after the Russian mathematician Boris Grigoryevich Galerkin (Борис Григорьевич Галёркин) (1871-1945), the weighing functions are the same as the basis functions:

$$\sum_{i=1}^{N} \int_a^b b_j(x) c_i L(b_i(x)) dx = \int_a^b b_j(x) f(x) dx, \qquad j = 1, \cdots, N \tag{H.24}$$

We thus have a linear system of N equations:

$$\begin{bmatrix} \int_a^b b_1 L(b_1) dx & \int_a^b b_1 L(b_2) dx & \cdots & \int_a^b b_1 L(b_N) dx \\ \int_a^b b_2 L(b_1) dx & \int_a^b b_2 L(b_2) dx & \cdots & \int_a^b b_2 L(b_N) dx \\ \vdots & \cdots & \ddots & \vdots \\ \int_a^b b_N L(b_1) dx & \int_a^b b_N L(b_2) dx & \cdots & \int_a^b b_N L(b_N) dx \end{bmatrix} \begin{bmatrix} c_1 \\ c_2 \\ \vdots \\ c_N \end{bmatrix} = \begin{bmatrix} \int_a^b b_1(x) f(x) dx \\ \int_a^b b_2(x) f(x) dx \\ \vdots \\ \int_a^b b_N(x) f(x) dx \end{bmatrix} \tag{H.25}$$

The entire procedure of approximating the solution of a linear equation as a linear combination of basis functions, and then minimizing the error residue by applying a weighing method is called 'Method of Moments'. Hence, the partial element equivalent circuit technique is a Moment Method.

End of intermezzo

So, let us 'weigh' equation (H.17) according to Galerkin, by multiplying it with a pulse function $P^V_{\gamma,m,l}$, corresponding to the l^{th} volume cell for the γ-direction on conductor m, and then integrating over this cell (cf. eq. H.24):

$$\frac{J_{\gamma,m,l}(t)A_{\gamma,m,l}l_m}{\sigma} + \sum_{k=1}^{K}\frac{1}{4\pi\epsilon}\left[\int_{V_{\gamma,m,l}}\frac{\partial}{\partial\gamma}\int_{S_k}\frac{\rho'(\vec{r'},t')}{R}dS'dV'_{\gamma,m,l}\right] +$$

$$\sum_{k=1}^{K}\sum_{n=1}^{N_{\gamma,k}}\frac{\mu}{4\pi}\left[\int_{V_{\gamma,m,l}}\int_{V_{\gamma,n,k}}\frac{\frac{\partial}{\partial t}J_{\gamma,n,k}(t_n)}{R}dV'_{\gamma,n,k}dV'_{\gamma,m,l}\right]$$

$$\approx A_{\gamma,m,l}l_mE_{i,\gamma,m,l}(t) \tag{H.26}$$

Where l_m is the length of the l^{th} cell. Also notice that in previous equation, the $\vec{r}$ disappeared from the arguments of $J_{\gamma,m,l}$ and $E_{i,\gamma,m,l}$ because of the integration over $V_{\gamma,m,l}$. Also, making use of $J_\gamma = I_\gamma/A_\gamma$, gives us:

$$\frac{I_{\gamma,m,l}(t)l_m}{\sigma} + \sum_{k=1}^{K}\frac{1}{4\pi\epsilon}\left[\int_{V_{\gamma,m,l}}\frac{\partial}{\partial\gamma}\int_{S_k}\frac{\rho'(\vec{r'},t')}{R}dS'dV'_{\gamma,m,l}\right] +$$

$$\sum_{k=1}^{K}\sum_{n=1}^{N_{\gamma,k}}\frac{\mu}{4\pi}\left[\frac{1}{A_{\gamma,n,k}}\int_{V_{\gamma,m,l}}\int_{V_{\gamma,n,k}}\frac{\frac{\partial}{\partial t}I_{\gamma,n,k}(t_n)}{R}dV'_{\gamma,n,k}dV'_{\gamma,m,l}\right]$$

$$\approx A_{\gamma,m,l}l_mE_{i,\gamma,m,l}(t) \tag{H.27}$$

Let us divide by the area of the cross-section of the l^{th} segment on the m^{th} conductor, perpendicular to direction γ, $A_{\gamma,m,l}$:

$$\frac{I_{\gamma,m,l}(t)l_m}{A_{\gamma,m,l}\sigma} + \sum_{k=1}^{K}\frac{1}{4\pi\epsilon}\left[\frac{1}{A_{\gamma,m,l}}\int_{V_{\gamma,m,l}}\frac{\partial}{\partial\gamma}\int_{S_k}\frac{\rho'(\vec{r'},t')}{R}dS'dV'_{\gamma,m,l}\right] +$$

$$\sum_{k=1}^{K}\sum_{n=1}^{N_{\gamma,k}}\frac{\mu}{4\pi}\left[\frac{1}{A_{\gamma,n,k}}\frac{1}{A_{\gamma,m,l}}\int_{V_{\gamma,m,l}}\int_{V_{\gamma,n,k}}\frac{\frac{\partial}{\partial t}I_{\gamma,n,k}(t_n)}{R}dV'_{\gamma,n,k}dV'_{\gamma,m,l}\right]$$

$$\approx l_mE_{i,\gamma,m,l}(t) \tag{H.28}$$

Let us now apply as similar procedure as for the third term of the left hand-side of previous equation on the second term:

$$\sum_{k=1}^{K}\frac{1}{4\pi\epsilon}\frac{1}{A_{\gamma,m,l}}\int_{V_{\gamma,m,l}}\frac{\partial}{\partial\gamma}\left[\int_{S_k}\frac{\rho'(\vec{r'},t')}{R}dS'\right]dV'_{\gamma,m,l}$$

$$\approx\sum_{k=1}^{K}\frac{1}{4\pi\epsilon}\frac{1}{A_{\gamma,m,l}}\int_{V_{\gamma,m,l}}\frac{\partial}{\partial\gamma}\left[\int_{S_k}\frac{1}{R}\left(\sum_{q=1}^{Q_k}P^S_{q,k}\rho'_{q,k}(t_q)\right)dS'\right]dV'_{\gamma,m,l}$$

$$=\sum_{k=1}^{K}\sum_{q=1}^{Q_k}\frac{1}{4\pi\epsilon}\frac{1}{A_{\gamma,m,l}}\int_{V_{\gamma,m,l}}\frac{\partial}{\partial\gamma}\left[\int_{S_k}P^S_{q,k}\rho'_{q,k}(t_q)\frac{1}{R}dS'\right]dV'_{\gamma,m,l}$$

$$=\sum_{k=1}^{K}\sum_{q=1}^{Q_k}\frac{1}{4\pi\epsilon}\frac{1}{A_{\gamma,m,l}}\int_{V_{\gamma,m,l}}\frac{\partial}{\partial\gamma}\left[\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{R}dS'_{q,k}\right]dV'_{\gamma,m,l}\qquad\text{(H.29)}$$

Here, $R=|\vec{r}-\vec{r'}|$, with $\vec{r'}$ the points of $S_{q,k}$ and with $\vec{r}$ the points of $V_{\gamma,m,l}$. Making use of

$$\begin{aligned}\int_{V_{\gamma,m,l}}\frac{\partial}{\partial\gamma}f(\gamma)dV'_{\gamma,m,l} &\approx l_m A_{\gamma,m,l}\left(\frac{f(\gamma+\frac{l_m}{2})-f(\gamma-\frac{l_m}{2})}{l_m}\right)\\ &= A_{\gamma,m,l}\left(f(\gamma+\frac{l_m}{2})-f(\gamma-\frac{l_m}{2})\right)\end{aligned}$$

equation (H.29) becomes:

$$\sum_{k=1}^{K}\sum_{q=1}^{Q_k}\frac{1}{4\pi\epsilon}\frac{1}{A_{\gamma,m,l}}\int_{V_{\gamma,m,l}}\frac{\partial}{\partial\gamma}\left[\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{R}dS'_{q,k}\right]dV'_{\gamma,m,l}$$

$$\approx\sum_{k=1}^{K}\sum_{q=1}^{Q_k}\frac{A_{\gamma,m,l}}{4\pi\epsilon A_{\gamma,m,l}}\left[\left(\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{R}dS'_{q,k}\right)\Bigg|_{\gamma+\frac{l_m}{2}}-\left(\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{R}dS'_{q,k}\right)\Bigg|_{\gamma-\frac{l_m}{2}}\right]$$

$$=\sum_{k=1}^{K}\sum_{q=1}^{Q_k}\frac{1}{4\pi\epsilon}\left[\left(\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{|\vec{r}-\vec{r'}|}dS'_{q,k}\right)\Bigg|_{\gamma+\frac{l_m}{2}}-\left(\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{|\vec{r}-\vec{r'}|}dS'_{q,k}\right)\Bigg|_{\gamma-\frac{l_m}{2}}\right]$$

$$=\sum_{k=1}^{K}\sum_{q=1}^{Q_k}\frac{1}{4\pi\epsilon}\left[\left(\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{|\vec{r}+\frac{l_m}{2}\vec{u}_\gamma-\vec{r'}|}dS'_{q,k}\right)-\left(\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{|\vec{r}-\frac{l_m}{2}\vec{u}_\gamma-\vec{r'}|}dS'_{q,k}\right)\right]$$

$$=\sum_{k=1}^{K}\sum_{q=1}^{Q_k}\frac{1}{4\pi\epsilon}\left[\left(\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{|\vec{r^+}-\vec{r'}|}dS'_{q,k}\right)-\left(\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{|\vec{r^-}-\vec{r'}|}dS'_{q,k}\right)\right]\qquad\text{(H.30)}$$

Vectors $\vec{r^+}$ and $\vec{r^-}$ are associated with the positive and the negative ends of the cell $V_{\gamma,m,l}$, respectively. With this result, eq. (H.28) becomes:

$$\frac{I_{\gamma,m,l}(t)l_m}{A_{\gamma,m,l}\sigma}+$$

$$\sum_{k=1}^{K}\sum_{q=1}^{Q_k}\frac{1}{4\pi\epsilon}\left[\left(\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{|\vec{r^+}-\vec{r'}|}dS'_{q,k}\right)-\left(\int_{S_{q,k}}\frac{\rho'_{q,k}(t_q)}{|\vec{r^-}-\vec{r'}|}dS'_{q,k}\right)\right]+$$

$$\sum_{k=1}^{K}\sum_{n=1}^{N_{\gamma,k}}\frac{\mu}{4\pi}\left[\frac{1}{A_{\gamma,n,k}}\frac{1}{A_{\gamma,m,l}}\int_{V_{\gamma,m,l}}\int_{V_{\gamma,n,k}}\frac{\frac{\partial}{\partial t}I_{\gamma,n,k}(t_n)}{R}dV'_{\gamma,n,k}dV'_{\gamma,m,l}\right]\approx l_m E_{i,\gamma,m,l}(t) \tag{H.31}$$

Manual for PCBParC

PCBParC is a software tool for Windows which collaborates with FastHenry and FastCap to extract a Spice-circuit modelling the metal tracks of a single-layered PCB-circuit on a dielectric substrate.

- PCBParC is free and open source software.
- PCBParC may be modified for personal use provided this license remains in force.
- PCBParC comes with no warranty whatsoever; not even the implied warranty of merchantability or fitness for a particular purpose.
- Any publications derived from the use of PCBParC must acknowledge PCBParC.
- PCBParC may not be redistributed without prior written permission.
- Modified versions of PCBParC, or works derived from PCBParC, may not be distributed without prior written permission.

The computer requirements are:

- Microsoft Windows XP or 7
- Matlab Compiler Runtime (MCR) or Matlab should be installed

- FastHenry and FastCap should be installed
- The country/language/number-settings on the computer must be set so that the point is used as the decimal separator and the comma is used as the separator for the thousands.

PCBParC is based on the following assumptions:

- The extracted Spice-circuit is either a quasi-static model or a full-wave model of the electric circuit.
- The PCB-tracks are either made of a Perfectly Electrically Conducting (PEC) material or of copper with a specific conductivity of $5.8108 \cdot 10^7$ S/m.
- The PCB-tracks have the shape of bars with a rectangular cross-section.
- If tracks intersect each other, this should occur at right angles (of 90°) or at angles of 180°.
- Only a single-layered PCB can be modelled.
- The coordinate system is a right-handed orthonormal set of xyz-axes, where the x-axis points from left to right and the y-axis points from the bottom to the top.
- It is not necessary to have a dielectric substrate. However, it can be present immediately underneath the PCB-tracks touching them, or at a certain distance underneath them. In this version of PCBParC, the substrate will be ignored in full-wave computations.
- There are only 999999 Spice nodes (including the internal ones) allowed.
- The skin- and proximity-effects are taken into account. Tracks are segmented in the width- and/or height-direction in FastHenry.
- The size of all the panels of the capacitive segmentation of the conductors and of the dielectric substrate in FastCap is approximately equal and is an input parameter.

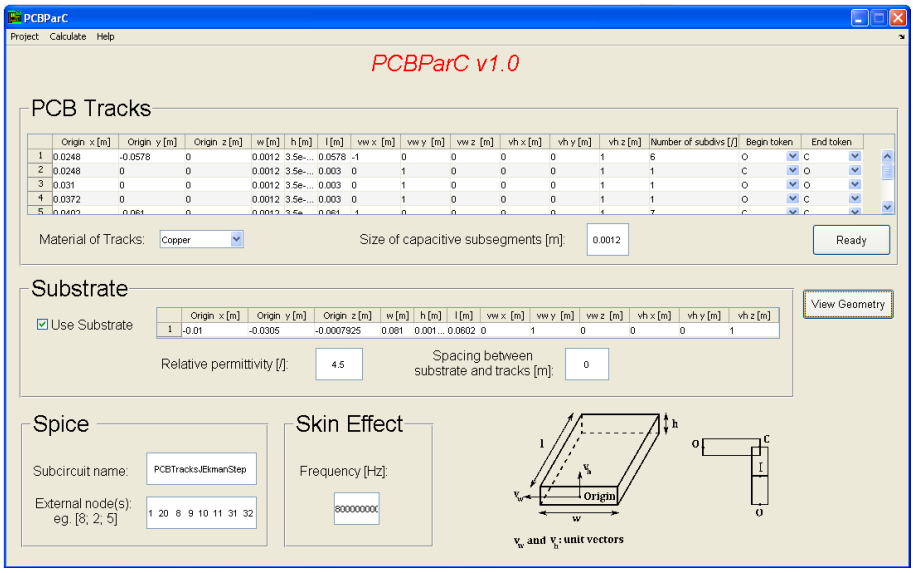


Figure I.1: PCBParC's main window.

I.1 The PCB Tracks panel

This panel is depicted in Fig. I.2. The table allows to input the metal PCB-tracks. Each row of the table specifies one track (= one bar).

- The columns 'Origin x', 'Origin y' and 'Origin z' specify respectively the x-, y-, and z-coordinates of a point in the middle of the starting plane of the bar (see Fig. I.3). Units=metres.
- The column 'w' specifies the width of a bar (see Fig. I.3). Units=metres.
- The column 'h' specifies the height of a bar (see Fig. I.3). Units=metres.
- The column 'l' specifies the length of a bar (see Fig. I.3). Units=metres.
- The columns 'vw x', 'vw y' and 'vw z' specify respectively the x-, y- and z-coordinates of the unit vector in the width-direction (see Fig. I.3). Units=metres.
- The columns 'vh x', 'vh y' and 'vh z' specify respectively the x-, y- and z-coordinates of the unit vector in the height-direction (see Fig. I.3). Units=metres.

- The column 'Number of subdivs' lets a user divide the bar in smaller segments, for FastHenry. This column specifies in how many smaller segments the bar should be divided.
- 'Begin Token' can be 'O', 'C' or 'I'. It is 'O' (for 'open') if the begin point of the bar is not connected to any other bar. It is 'C' (for 'corner') if the begin point of the bar is connected to another bar, at a right angle. It is 'I' (for 'inner') if the begin point of the bar is connected to an other bar, which is parallel to it. The column 'End Token' specifies in an analogous way the manner in which the end point of a bar is connected to another bar.

It is possible, instead of using the graphical user interface for creating the project, to make a Matlab mat-file containing a few variables, specifying your geometry and your project. The first 13 columns of the table of the PCB Tracks panel can be specified in the Nx13-matrix **structuur**, with N the number of copper bars. The last two columns of the table can be specified in the Nx2-cell matrix **beginendtokens**, containing for each element one of the characters 'O', 'C' or 'I'.

The coordinate system is a right-handed orthonormal set of xyz-axes, where the x-axis points from left to right and the y-axis points from the bottom to the top.

It is furthermore important to know that the geometry of the metal bars should be input just like one does in FastHenry.

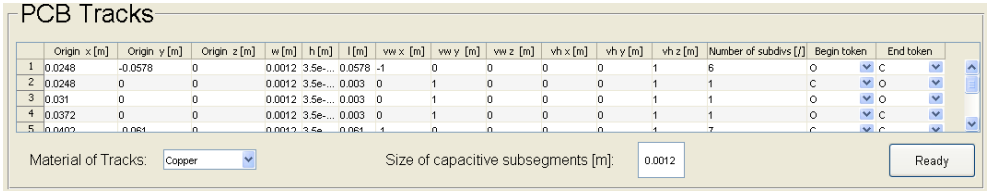


Figure I.2: PCB Tracks panel.

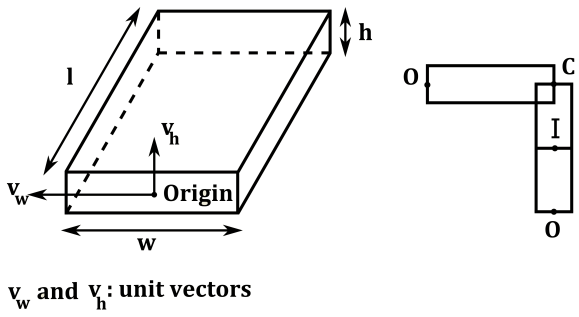


Figure I.3: Geometry of the bars.

The pull-down menu 'Material of Tracks' specifies whether the tracks are made from copper (with a conductivity of 5.8108e7 S/m), or from a perfectly electrically conductive material. If one wishes not to use the GUI for creating one's project, but specify it with a mat-file, use the string variable **materialtracks**, which can have values 'PEC' or 'Copper'.

The box 'Size of capacitive subsegments' specifies, in metres, the size of the edges of the (approximately) square panels in which the outer faces of the copper PCB-tracks are subdivided into for the FastCap-calculation. If one wishes not to use the GUI for creating one's project, but specifying it with a mat-file, use the scalar variable **divsize**.

When using the GUI for inputting the geometry, do not forget to click on the 'Ready'-button after the geometry of the metal tracks has been specified!

I.2 The Substrate panel and the button 'View Geometry'

The Substrate panel (Fig. I.4) lets a user input a dielectric substrate underneath the metal PCB tracks. However, it is also possible not to have a substrate present. The checkbox 'Use substrate' specifies whether a substrate should or should not be used. If one wishes not to use the GUI for creating one's project, but specify it with a mat-file, use the scalar variable **usesubs**. usesubs can have the values 1 (if a substrate is present) or 0 (if there is no substrate). The table (consisting of a single row) lets a user specify the dimensions of a rectangular shaped dielectric substrate in an analogous manner as the first 12

columns of the PCB Tracks table allow the specification of the geometry of the metal bars. Its Matlab variable is the 1x12-matrix **substrate**. The box 'relative permittivity' specifies the relative electric permittivity (dimensionless) of the dielectric substrate. Its Matlab-variable is the scalar **epsilon_r**. The box 'spacing between substrate and tracks' specifies, in metres, an extra separation distance between the bottom of the copper tracks and the top face of the dielectric substrate. Its Matlab-variable is the scalar **depth**.

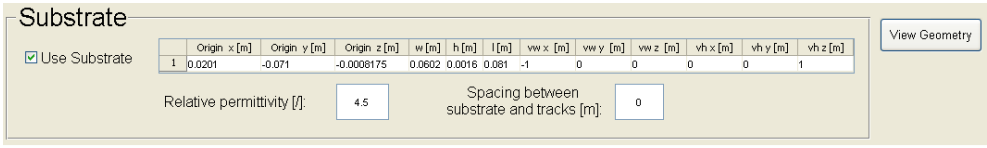


Figure I.4: Substrate panel and the button 'View Geometry'.

The button 'View Geometry' can be clicked to see the geometry of the metal bars and the substrate, the segmentation of the bars in smaller elements and the attribution of Spice node names to the end points of the elements.

I.3 Spice panel

The Spice panel (Fig. I.5) contains two boxes. One ('subcircuit name') for specifying the name of the Spice-subcircuit of the PCB-circuit which is to be created. Its Matlab-variable is the string variable **modelnaam**. The other one ('external node(s)') contains the column vector of the nodes which are externally accessible in the subcircuit. Its content should be specified such as in Matlab: for instance [node1;node2;node3], where node1, node2 and node3 are numeric node numbers. Remark that angle brackets are used and that the node numbers are separated from each other with semicolons. The Matlab-variable corresponding to this box is the vector variable **externalspicenodes**.

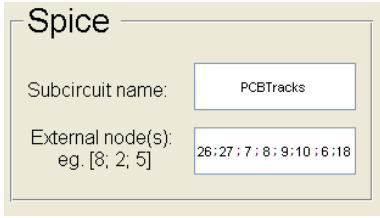


Figure I.5: Spice panel.

I.4 Skin-effect panel

The skin-effect panel (Fig. I.6) contains a box for specifying the frequency (in Hertz) of the current which flows through the PCB-tracks and is subject to the skin-effect. The Matlab-variable corresponding to this box is the scalar variable **frequency**.

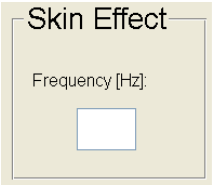


Figure I.6: Skin-effect panel.

I.5 Running PCBParC

Click on the menu 'Calculate', 'Generate Spice Model'. You can then choose if a quasi-static or full-wave model is to be extracted. If a full-wave model is to be extracted, it is possible to either use a series connection of voltage sources to model the capacitive interactions or to use a parallel connection of current sources. Then, the following process takes place:

1. The file *FH_input.inp* is created in the project directory, containing instructions for running FastHenry.
2. The visual basic script file *fhdriv.vbs* is copied to the project directory and executed in order to run FastHenry.
3. FastHenry is executed.
4. Upon finishing, FastHenry dumps the file *Zc.mat*, containing the [R]+jω[L]-matrix, in the project directory. ω is the pulsation, corresponding with a frequency of 100 MHz.
5. This file (*Zc.mat*) is next written in a slightly different format (file *Zc_formatted.txt*) in order to facilitate the data reading.
6. The R- and L-matrices are written in the project directory in mat-files *R.mat* and *L.mat*.

7. The directory 'fastCapInput' is created in the project directory. In this directory, the .qui-files specifying the coordinates of the panels on the outer surface of the metal conducting bars, are stored. Also, the .lst-file, needed for running FastCap, is stored in this directory.

8. The .qui-files for each conductor are made and stored in the directory 'fastCapInput'.

9. If a substrate is present and it touches the copper or PEC bars, then a triangular meshing procedure is started. Using the Matlab programme mesh2D, the top face of the substrate is meshed around the copper conductors. The size of the triangles corresponds to the value of the **divsize** variable (see Section I.1). The coordinates of the points of the triangles are written to *substrate.qui*. For the other five planes of the substrate-bar, a rectangular meshing is performed. The coordinates of the points of these rectangles are appended to the same file, *substrate.qui*.

10. The list-file *fastCapListFile.lst*, needed for running FastCap, is created and written to the directory 'fastCapInput'.

11. The visual basic script file *fcdriv.vbs* is copied to the directory 'fastCapInput'. It is called, thereby running FastCap.

12. FastCap is executed.

13. When FastCap finishes, a Windows pop-up window reveals the success or failure of the process. A return code of 0 signifies success. An other number signifies failure. This errorcode is written to the file *errorcode_fc.txt* in the directory 'fastCapInput'.

14. The short-circuit capacitance matrix returned by FastCap is written to the mat-file *Cs.mat* and to the text-file *Cformatted.txt* in the directory 'fastCapInput'.

15. The short-circuit capacitance matrix is converted to the real capacitance matrix, written to the mat-file *C.mat* in the directory 'fastCapInput'.

16. If a full-wave model extraction is chosen, the delays between the inductive cells are calculated, as are the delays between the capacitive cells.

17. The Spice-model of the PCB-circuit is written -in Spice format- to the file *spiceFile.txt* in the project directory.

18. For full-wave model extraction, the main constituents of the PEEC system matrix (eq. (4.27)) are then written to the file *systemmatrix.mat* in the project directory. They can for instance be used to solve the system or for stability analysis.

19. The current and charge elements are finally written to the mat-file *geometry.mat* in the project directory. This is done for a future extension of PCBParC, which will automatically allow the calculation of electromagnetic fields around the electric circuit.

J

Derivation of the Jefimenko equations

The electric field $\vec{E}(\vec{r},t)$ at a certain point in space $\vec{r}$, and at time instance t, is given by [Harr 68]:

$$\vec{E}(\vec{r},t) = -\vec{\nabla}\phi(\vec{r},t) - \frac{\partial \vec{A}(\vec{r},t)}{\partial t} \tag{J.1}$$

The magnetic induction $\vec{B}(\vec{r},t)$ at a certain point in space $\vec{r}$, and at time instance t, is given by [Harr 68]:

$$\vec{B}(\vec{r},t) = \vec{\nabla} \times \vec{A}(\vec{r},t) \tag{J.2}$$

where ϕ is the electric scalar potential and $\vec{A}$ is the magnetic vector potential. These two potentials are functions of the charges and currents, present in a volume V, respectively. More precisely, they can be written as follows [Harr 68]:

$$\phi(\vec{r},t) = \frac{1}{4\pi\epsilon}\int_V \frac{\rho(\vec{r'},t-R/v)}{R}dV' \tag{J.3}$$

$$\vec{A}(\vec{r},t) = \frac{\mu}{4\pi}\int_V \frac{\vec{J}(\vec{r'},t-R/v)}{R}dV' \tag{J.4}$$

where ϵ and μ are the permittivity and permeability of the medium where the fields are calculated. The assumption in writing previous equations is that

this medium is homogeneous and isotropic. $\vec{r'}$ is a point in the volume V. ρ is the volume charge density (units: C/m^3). $\vec{R}$ is the vector which points from the source point to the observation point: $\vec{R} = \vec{r} - \vec{r'}$. v is the speed of electromagnetic waves in the medium surrounding the charges and currents. These potentials, ϕ and $\vec{A}$, are also called 'retarded potentials'. Let us now plug the expressions for the retarded potentials into eqs. (J.1) and (J.2). We shall from now on denote the retarded time $t - R/v$ by t_r.

J.1 Magnetic induction

Making use of $\vec{\nabla} \times \left(\psi \vec{A}\right) = \psi \vec{\nabla} \times \vec{A} + \vec{\nabla}\psi \times \vec{A}$ and the fact that $\vec{A} \times \vec{B} = -\vec{B} \times \vec{A}$, we have:

$$\vec{\nabla} \times \vec{A}(\vec{r}, t) = \frac{\mu}{4\pi} \int_V \left[\frac{1}{R} \left(\vec{\nabla} \times \vec{J} \right) - \vec{J} \times \vec{\nabla} \left(\frac{1}{R} \right) \right] dV' \tag{J.5}$$

Now, calculate $\vec{\nabla} \times \vec{J}$, component by component:

$$\begin{aligned} \left(\vec{\nabla} \times \vec{J} \right)_x &= \frac{\partial J_z}{\partial y} - \frac{\partial J_y}{\partial z} = \frac{\partial J_z}{\partial t}\frac{\partial t_r}{\partial y} - \frac{\partial J_y}{\partial t}\frac{\partial t_r}{\partial z} \\ &= \frac{\partial J_z}{\partial t}\left(-\frac{1}{v}\frac{\partial R}{\partial y} \right) - \frac{\partial J_y}{\partial t}\left(-\frac{1}{v}\frac{\partial R}{\partial z} \right) = \frac{1}{v}\left[\frac{\partial \vec{J}}{\partial t} \times \left(\vec{\nabla} R \right) \right]_x \end{aligned}$$

But, with $R = \sqrt{(x-x')^2 + (y-y')^2 + (z-z')^2}$ we have,

$$\begin{aligned} \vec{\nabla} R &= \vec{\nabla} |\vec{r} - \vec{r'}| \\ &= \frac{\partial R}{\partial x}\vec{e}_x + \frac{\partial R}{\partial y}\vec{e}_y + \frac{\partial R}{\partial z}\vec{e}_z \\ &= \vec{e}_x \left(\frac{1}{2}\frac{2(x-x')}{R} \right) + \vec{e}_y \left(\frac{1}{2}\frac{2(y-y')}{R} \right) + \vec{e}_z \left(\frac{1}{2}\frac{2(z-z')}{R} \right) \\ &= \frac{1}{R}\left(x\vec{e}_x - x'\vec{e}_x + y\vec{e}_y - y'\vec{e}_y + z\vec{e}_z - z'\vec{e}_z \right) \\ &= \frac{1}{R}\left(\vec{r} - \vec{r'} \right) = \frac{\vec{R}}{R} = \vec{e}_R \end{aligned}$$

where $\vec{e}_R$ is the unit vector in the $\vec{r} - \vec{r'}$-direction. We have:

$$\left(\vec{\nabla} \times \vec{J} \right)_x = \frac{1}{v}\left[\frac{\partial \vec{J}}{\partial t} \times \left(\vec{\nabla} R \right) \right]_x = \frac{1}{v}\left[\frac{\partial \vec{J}}{\partial t} \times \left(\vec{e}_R \right) \right]_x \tag{J.6}$$

and an analogue equation holds for the y- and z-component of $\vec{\nabla} \times \vec{J}$. Furthermore, we have:

$$\vec{\nabla}\left(\frac{1}{R}\right) = \vec{\nabla}\left(\frac{1}{|\vec{r} - \vec{r'}|}\right) = \frac{-1}{R^2}\left(\vec{\nabla}R\right) = -\frac{1}{R^2}\vec{e}_R \tag{J.7}$$

Using the identities (J.6) and (J.7) in eq. (J.5), we obtain the first Jefimenko equation:

$$\boxed{\vec{B}(\vec{r},t) = \frac{\mu}{4\pi}\int_V \left[\frac{\vec{J}(\vec{r'},t_r)}{R^2} + \frac{\frac{\partial \vec{J}}{\partial t}(\vec{r'},t_r)}{vR}\right] \times \vec{e}_R dV'} \tag{J.8}$$

This is a generalization of the Biot-Savart law for time-dependent currents.

J.2 Electric field

According to (J.1), we need to calculate two terms for $\vec{E}$: $\vec{\nabla}\phi$ and $\frac{\partial \vec{A}}{\partial t}$. The second term is easy to calculate:

$$\frac{\partial \vec{A}}{\partial t} = \frac{\mu}{4\pi}\int_V \left[\frac{\frac{\partial \vec{J}}{\partial t}}{R}\right] dV' \tag{J.9}$$

Let us now calculate the gradient of the scalar potential. Making use of the identity $\vec{\nabla}(fg) = f\vec{\nabla}g + g\vec{\nabla}f$, we have:

$$\begin{aligned}\vec{\nabla}\phi &= \vec{\nabla}\left(\frac{1}{4\pi\epsilon}\int_V \frac{\rho(\vec{r'},t_r)}{R}dV'\right) \\ &= \frac{1}{4\pi\epsilon}\int_V \left[\left(\vec{\nabla}\rho\right)\frac{1}{R} + \rho\vec{\nabla}\left(\frac{1}{R}\right)\right] dV'\end{aligned} \tag{J.10}$$

and

$$\vec{\nabla}\rho = \vec{\nabla}\rho(\vec{r'},t_r) = \frac{\partial \rho}{\partial t}\vec{\nabla}t_r = \frac{\partial \rho}{\partial t}\cdot\frac{-1}{v}\vec{\nabla}R \tag{J.11}$$

In Section J.1, we saw that $\vec{\nabla}R = \vec{e}_R$ and $\vec{\nabla}\left(\frac{1}{R}\right) = \frac{-1}{R^2}\vec{e}_R$. Therefore, using eqs. (J.9) and (J.10), and the fact that $v^2 = 1/(\mu\epsilon)$, we find for the electric field:

$$\boxed{\vec{E}(\vec{r},t) = \frac{1}{4\pi\epsilon}\int_V \left[\frac{\rho(\vec{r'},t_r)}{R^2}\vec{e}_R + \frac{\frac{\partial \rho}{\partial t}(\vec{r'},t_r)}{vR}\vec{e}_R - \frac{\frac{\partial \vec{J}}{\partial t}(\vec{r'},t_r)}{v^2R}\right] dV'} \tag{J.12}$$

This is the second Jefimenko equation. It is a generalization of Coulomb's law for moving charges.

K

Electric and magnetic field between two wires

K.1 Problem description

Two cylindrical wires, each conducting a DC current I are parallel to the z-axis (Fig. 5.1). They are infinitely long. The first wire is located at $x = -d$ and conducts the current in the positive z-direction. The other wire is located at $x = d$ and conducts the current in the negative z-direction. The left wire has a potential $-V_1$ and the right wire V_1. The scalar potential, the electric and the magnetic field in the region outside the conductors must be determined. The cross-section of the right wire is bounded by a circle, called C_1. The electric potential ϕ is given by the Laplace equation:

$$\nabla^2 \phi = 0 \tag{K.1}$$

This will be solved using an appropriate coordinate system: bipolar coordinates.

K.2 Bipolar coordinates

The bipolar coordinate system is defined as ($\tau \in [-\infty, \infty]$ and $\sigma \in [0, 2\pi]$):

$$\begin{cases} x = \alpha \dfrac{\sinh \tau}{\cosh \tau - \cos \sigma} & \text{(K.2)} \\ y = \alpha \dfrac{\sin \sigma}{\cosh \tau - \cos \sigma} & \text{(K.3)} \end{cases}$$

The curves of constant σ form non-concentric circles with origin point on the y-axis. The radius decreases as σ increases in the interval $[0, \pi/2]$ and increases again with increasing σ in the interval $[\pi/2, \pi]$:

$$x^2 + (y - \alpha \cot \sigma)^2 = \frac{\alpha^2}{\sin^2 \sigma} \tag{K.4}$$

The curves of constant τ form non-concentric circles with origin point on the x-axis and decreasing radius as τ increases from 0 to ∞:

$$(x - \alpha \coth \tau)^2 + y^2 = \frac{\alpha^2}{\sinh^2 \tau} \tag{K.5}$$

These circles are depicted in Fig. K.1. For the problem of determining the

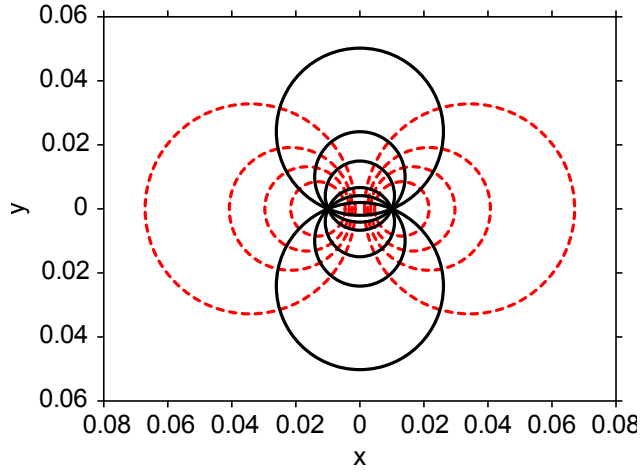


Figure K.1: Bipolar coordinate system, circles of constant τ (dashed lines) and circles of constant σ (solid lines).

electric scalar potential in the region outside the two wires, also the boundary conditions are rewritten in terms of bipolar coordinates.

K.3 First boundary condition: $\phi = 0$ on the y-axis

The y-axis has the equation $x = 0$. Thus, according to (K.2), this corresponds to points in the (τ, σ)-plane with $\tau = 0$.

K.4 Second boundary condition: $\phi = V_1$ on the circumference of the circle C_1

The circle C_1, with origin point $(0, d)$ and radius a, coincides with a circle of constant τ (cf. (K.5)), if

$$\begin{cases} d = \alpha \coth \tau \\ a = \frac{\alpha}{\sinh \tau} \end{cases} \tag{K.6}$$

From this, it follows that:

$$d = \alpha \coth \tau = \underbrace{\frac{\alpha}{\sinh \tau}}_{=a} \cosh \tau = a \cosh \tau$$

Now call the τ for which this circle C_1 is defined, τ_c. The relationship $\cosh \tau_c = d/a$ holds, and C_1 is thus defined by the single τ-coordinate:

$$\tau_c = \cosh^{-1} \frac{d}{a} \tag{K.7}$$

α can also be calculated from the second equation of (K.6):

$$a^2 = \frac{\alpha^2}{\sinh^2 \tau_c} = \frac{\alpha^2}{\cosh^2 \tau_c - 1} = \frac{\alpha^2}{\left(\frac{d^2 - a^2}{a^2}\right)}$$

Thus:

$$\alpha = \sqrt{d^2 - a^2} \tag{K.8}$$

K.5 Formulation of the problem in bipolar coordinates

The scalar potential ϕ has to obey the Laplace partial differential equation in bipolar coordinates:

$$\nabla^2 \phi = \frac{1}{\alpha^2} (\cosh \tau - \cos \sigma)^2 \left(\frac{\partial^2 \phi}{\partial \sigma^2} + \frac{\partial^2 \phi}{\partial \tau^2} \right) = 0 \tag{K.9}$$

with boundary conditions:

$$\phi(\sigma, \tau = 0) = 0, \qquad \sigma \in [0, 2\pi] \tag{K.10}$$

$$\phi(\sigma, \tau = \tau_c) = V_1, \qquad \sigma \in [0, 2\pi] \tag{K.11}$$

where ϕ is a periodic function in σ with a period equal to 2π, and τ_c as defined in (K.7).

K.6 Solution of the Laplace equation with boundary conditions

The method of separation of variables is applied. This means that the solution for the potential ϕ is written as the product of single-variable functions:

$$\phi(\sigma, \tau) = S(\sigma)T(\tau) \tag{K.12}$$

When this equation is filled into the Laplace equation (K.9) a system of two differential equations must be solved:

$$\begin{cases} S''(\sigma) - kS(\sigma) = 0 & \text{(K.13)} \\ T''(\tau) + kT(\tau) = 0 & \text{(K.14)} \end{cases}$$

This has different solutions according to the sign of k.

K.6.1 Case $k = 0$

If $k = 0$ then (K.13) and (K.14) become

$$S''(\sigma) = 0$$

$$T''(\tau) = 0$$

The solutions for which are:

$$T(\tau) = A_0 + A_1\tau \tag{K.15}$$

$$S(\sigma) = B_0 + B_1\sigma \tag{K.16}$$

But because $S(\sigma)$ is periodic in σ, B_1 must be equal to 0. It thus follows that:

$$T(\tau) = A_0 + A_1\tau \tag{K.17}$$

$$S(\sigma) = B_0 \tag{K.18}$$

K.6.2 Case $k > 0$

If $k > 0$, then the general particular solution of (K.13) is:

$$S(\sigma) = C_1 \cos(\sqrt{k}\sigma) + C_2 \sin(\sqrt{k}\sigma)$$

However, because $S(\sigma)$ is periodic in σ with period 2π, $\sqrt{k} = n$ where n is a whole number, larger than 0. The solution for $S(\sigma)$ is thus:

$$S(\sigma) = D_n \cos(n\sigma) + E_n \sin(n\sigma) \tag{K.19}$$

The solution for $T(\tau)$ is:

$$T(\tau) = F_n \cosh(n\tau) + G_n \sinh(n\tau) \tag{K.20}$$

K.6.3 Case $k < 0$

If $k < 0$ then the general solution of (K.13) is:

$$S(\sigma) = C_3 \cosh(\sqrt{k}\sigma) + C_4 \sinh(\sqrt{k}\sigma)$$

However, because $S(\sigma)$ is a periodic function in σ, this solution is not feasible. Only non-negative k's can be allowed.

K.6.4 Solution of ϕ

The scalar potential $\phi(\sigma, \tau)$ is a linear combination of the solutions for every k-value and has the form:

$$\phi(\sigma,\tau) = (A_0+A_1\tau)(B_0)+\sum_{n=1}^{\infty}(D_n\cos(n\sigma)+E_n\sin(n\sigma))(F_n\cosh(n\tau)+G_n\sinh(n\tau)) \tag{K.21}$$

The remaining boundary conditions (K.10) and (K.11) are now imposed:
Use of boundary condition (K.10)
The potential is zero for τ equal to zero:

$$\phi(\sigma, \tau = 0) = A_0B_0 + \left(\sum_{n=1}^{\infty} F_n(D_n \cos(n\sigma) + E_n \sin(n\sigma))\right) = 0$$

This is a Fourier series of the constant function 0, the coefficients of which are:

$$A_0 B_0 = 0 \tag{K.22}$$

$$F_n D_n = 0 \qquad \forall n \geq 1 \tag{K.23}$$

$$F_n E_n = 0 \qquad \forall n \geq 1 \tag{K.24}$$

Hence, ϕ can be simplified and is:

$$\phi(\sigma, \tau) = A_1 B_0 \tau + \sum_{n=1}^{\infty} (D_n \cos(n\sigma) + E_n \sin(n\sigma))(G_n \sinh(n\tau)) \tag{K.25}$$

Use of boundary condition (K.11)
Imposing boundary condition (K.11) on (K.25), leads to:

$$\phi(\sigma, \tau = \tau_c) = A_1 B_0 \tau_c + \sum_{n=1}^{\infty} (D_n \cos(n\sigma) + E_n \sin(n\sigma))(G_n \sinh(n\tau_c)) = V_1$$

This is a Fourier series of the constant function V_1, the coefficients of which are thus:

$$A_1 B_0 \tau_c = V_1 \tag{K.26}$$

$$G_n D_n = 0 \qquad \forall n \geq 1 \tag{K.27}$$

$$G_n E_n = 0 \qquad \forall n \geq 1 \tag{K.28}$$

Hence, ϕ can be simplified, is independent of σ and is:

$$\boxed{\phi(\tau) = \frac{V_1}{\tau_c} \tau} \tag{K.29}$$

K.7 Expressing the scalar potential in Cartesian coordinates

Making use of (K.5), and the identity $\cosh^2\tau - \sinh^2\tau = 1$ we get:

$$\begin{aligned}(x-\alpha\coth\tau)^2+y^2 &= \frac{\alpha^2}{\sinh^2\tau}\\ &= \frac{\alpha^2}{\sinh^2\tau}.(\cosh^2\tau-\sinh^2\tau)\\ &= \alpha^2\coth^2\tau-\alpha^2\end{aligned}$$

$$\Downarrow$$

$$x^2-2\alpha x\coth\tau+\alpha^2\coth^2\tau+y^2+\alpha^2-\alpha^2\coth^2\tau=0$$

$$\Longrightarrow \coth\tau=\frac{x^2+y^2+\alpha^2}{2\alpha x}$$

And thus:

$$\tau=\tanh^{-1}\left(\frac{2\alpha x}{x^2+y^2+\alpha^2}\right) \tag{K.30}$$

The complete solution for the scalar potential in Cartesian coordinates is thus:

$$\begin{aligned}\phi(x,y) &= \frac{V_1}{\cosh^{-1}\frac{d}{a}}\tanh^{-1}\left(\frac{2x\sqrt{d^2-a^2}}{x^2+y^2+d^2-a^2}\right)\\ &= \frac{V_1}{\cosh^{-1}\frac{d}{a}}\ln\sqrt{\frac{x^2+y^2+\alpha^2+2\alpha x}{x^2+y^2+\alpha^2-2\alpha x}}\end{aligned}$$

$$\boxed{\phi(x,y)=\frac{V_1}{\ln\left(\frac{d}{a}+\sqrt{\frac{d^2}{a^2}-1}\right)}\ln\sqrt{\frac{(x+\sqrt{d^2-a^2})^2+y^2}{(x-\sqrt{d^2-a^2})^2+y^2}}} \tag{K.31}$$

K.8 Electric field

The electric field outside the two conducting wires, is thus:

$$\vec{E}(x,y)=-\vec{\nabla}\phi \tag{K.32}$$

$$\vec{E} = \frac{2(x^2 - d^2 + a^2 - y^2)\sqrt{d^2 - a^2}V_1.\vec{e}_x + 4V_1 xy\sqrt{d^2 - a^2}.\vec{e}_y}{((x + \sqrt{d^2 - a^2})^2 + y^2)\ln\left(\frac{d}{a} + \sqrt{\frac{d^2}{a^2} - 1}\right)((x - \sqrt{d^2 - a^2})^2 + y^2)} \tag{K.33}$$

K.9 Magnetic field

A DC current I flows in the positive z-direction in the wire at $x = -d$, and a DC current of I flows in the negative z-direction in the wire at $x = d$.

Call H_1 the magnetic field outside the two conductors, produced by the conductor at $x = -d$ and H_2 the magnetic field outside the two conductors, produced by the conductor at $x = d$. We have:

$$H_1 = \frac{I}{2\pi\sqrt{(x + d)^2 + y^2}} \tag{K.34}$$

$$H_2 = \frac{I}{2\pi\sqrt{(-x + d)^2 + y^2}} \tag{K.35}$$

K.9.1 Magnetic field in the region between the two wires: $-d \leq x \leq d$

With θ the angle between the x-axis starting at $(-d, 0)$ and going to infinity and the line from $(-d, 0)$ to (x, y) and γ the angle between the x-axis starting at $(d, 0)$ and going to infinity and the line from $(d, 0)$ to (x, y), we have:

$$\theta = \arctan\frac{y}{x + d} \tag{K.36}$$

$$\gamma = \arctan\frac{y}{-x + d} \tag{K.37}$$

and

$$\vec{H} = -H_1 \sin\theta\vec{e}_x + H_1 \cos\theta\vec{e}_y + H_2 \sin\gamma\vec{e}_x + H_2 \cos\gamma\vec{e}_y$$

Making use of the identities $\sin(\arctan(x)) = x/\sqrt{1 + x^2}$ and $\cos(\arctan(x)) = 1/\sqrt{1 + x^2}$, we obtain for the magnetic field outside the two wires, neglecting the small Hall-effect due to which the current density is not exactly constant in

each wire:

$$\begin{aligned}\vec{H}(x,y) &= \frac{Iy\vec{e}_x}{2\pi}\left(\frac{-1}{(x+d)^2+y^2}+\frac{1}{(x-d)^2+y^2}\right)+\\ &\quad \frac{I\vec{e}_y}{2\pi}\left(\frac{(x+d)}{(x+d)^2+y^2}+\frac{-(x-d)}{(x-d)^2+y^2}\right)\end{aligned} \tag{K.38}$$

We can see that inside this region, the dot product of the electric and the magnetic field is equal to:

$$\vec{E}.\vec{H} = \frac{4Ida^2V_1xy\sqrt{d^2-a^2}/\left(\pi\ln\left(\frac{d}{a}+\sqrt{\frac{d^2}{a^2}-1}\right)\right)}{((x+d)^2+y^2)((x-d)^2+y^2)((x+\sqrt{d^2-a^2})^2+y^2)((x-\sqrt{d^2-a^2})^2+y^2)} \tag{K.39}$$

This means that the electric and magnetic fields are not orthogonal in this region, except on the x- and y-axes.

K.9.2 Magnetic field in the region for which $x \leq -d$

With θ the angle between the x-axis starting at $(-d,0)$ and going to minus infinity and the line from $(-d,0)$ to (x,y) and γ the angle between the x-axis starting at $(d,0)$ and going to minus infinity and the line from $(d,0)$ to (x,y), we have:

$$\theta = \arctan\frac{-y}{x+d} \tag{K.40}$$

$$\gamma = \arctan\frac{y}{-x+d} \tag{K.41}$$

and

$$\vec{H} = -H_1\sin\theta\vec{e}_x - H_1\cos\theta\vec{e}_y + H_2\sin\gamma\vec{e}_x + H_2\cos\gamma\vec{e}_y \tag{K.42}$$

Making use of the identities $\sin(\arctan(x)) = x/\sqrt{1+x^2}$ and $\cos(\arctan(x)) = 1/\sqrt{1+x^2}$, we can again express the magnetic field in Cartesian coordinates. However, the expression is so long that for numerically evaluating it, we recommend that equation (K.42) is used. The dot product of the electric and the magnetic field can again be calculated. It is never zero in this region except on the x-axis. This means that the electric and magnetic fields are not orthogonal in this region, except on the x-axis.

K.9.3 Magnetic field in the region for which $x \geq d$

With θ the angle between the x-axis starting at $(-d, 0)$ and going to plus infinity and the line from $(-d, 0)$ to (x, y) and γ the angle between the x-axis starting at $(d, 0)$ and going to plus infinity and the line from $(d, 0)$ to (x, y), we have:

$$\theta = \arctan \frac{y}{x+d} \tag{K.43}$$

$$\gamma = \arctan \frac{y}{x-d} \tag{K.44}$$

and

$$\vec{H} = -H_1 \sin\theta \vec{e}_x + H_1 \cos\theta \vec{e}_y + H_2 \sin\gamma \vec{e}_x - H_2 \cos\gamma \vec{e}_y \tag{K.45}$$

Making use of the identities $\sin(\arctan(x)) = x/\sqrt{1+x^2}$ and $\cos(\arctan(x)) = 1/\sqrt{1+x^2}$, we can again express the magnetic field in Cartesian coordinates. However, the expression is so long that for numerically evaluating it, we recommend that equation (K.45) is used. The dot product of the electric and the magnetic field can again be calculated. It is never zero in this region except on the x-axis. This means that the electric and magnetic fields are not orthogonal in this region, except on the x-axis.

K.10 Surface charges on the wires

The surface density of the free charges on the surface of the right wire, centred around $x = d$, is σ_R, and is equal to ϵ_0 times the normal component of the electric field, perpendicular to the circle C_1. Here, ϵ_0 is the permittivity of vacuum. The surface density of the charges on the surface of the left wire is then, by symmetry, the mirrored image and the negative of σ_R. Let us determine σ_R. We choose a polar coordinate system (r, β) (Fig. K.2) where r is the distance from $(x, y) = (d, 0)$ to the observed point, and β is the angle between the x-axis, pointing from $(x, y) = (d, 0)$ to infinity and the line from $(x, y) = (d, 0)$ to the observed point. We have, for points on circle C_1, with $\beta \in [0, 2\pi]$:

$$\begin{cases} x = d + a\cos\beta, & \text{(K.46)} \\ y = a\sin\beta & \text{(K.47)} \\ \vec{e}_x = \cos\beta \vec{e}_r - \sin\beta \vec{e}_\beta & \text{(K.48)} \\ \vec{e}_y = \sin\beta \vec{e}_r + \cos\beta \vec{e}_\beta & \text{(K.49)} \end{cases}$$

Making these substitutions, we find a very simple form for the radial component

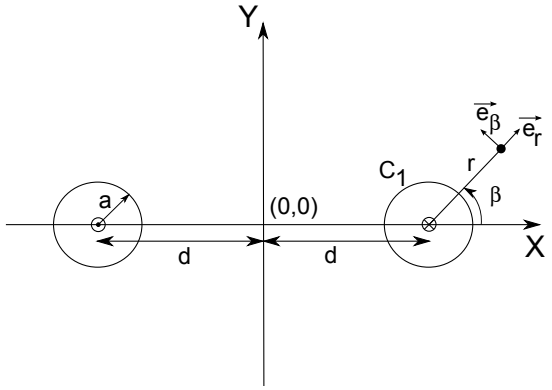


Figure K.2: Polar coordinate system, used for determining the surface charge density.

of the electric field:

$$E_r(r=a,\beta) = \frac{V_1\sqrt{d^2-a^2}}{a(d+a\cos\beta)\ln\left(\frac{d}{a}+\sqrt{\frac{d^2}{a^2}-1}\right)}$$

Hence, the surface charge density ($[C/m^2]$) is:

$$\sigma = \epsilon_0 E_r(r=a,\beta) = \frac{\epsilon_0 V_1\sqrt{d^2-a^2}}{a(d+a\cos\beta)\ln\left(\frac{d}{a}+\sqrt{\frac{d^2}{a^2}-1}\right)} \tag{K.50}$$

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List of Publications

All publications are available at: http://www.esat.kuleuven.be/electa
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